

GA102 GF SKU P-BOARD

370W, 7.4inch STD PCB, 320b, GDDR6x x16 10GB

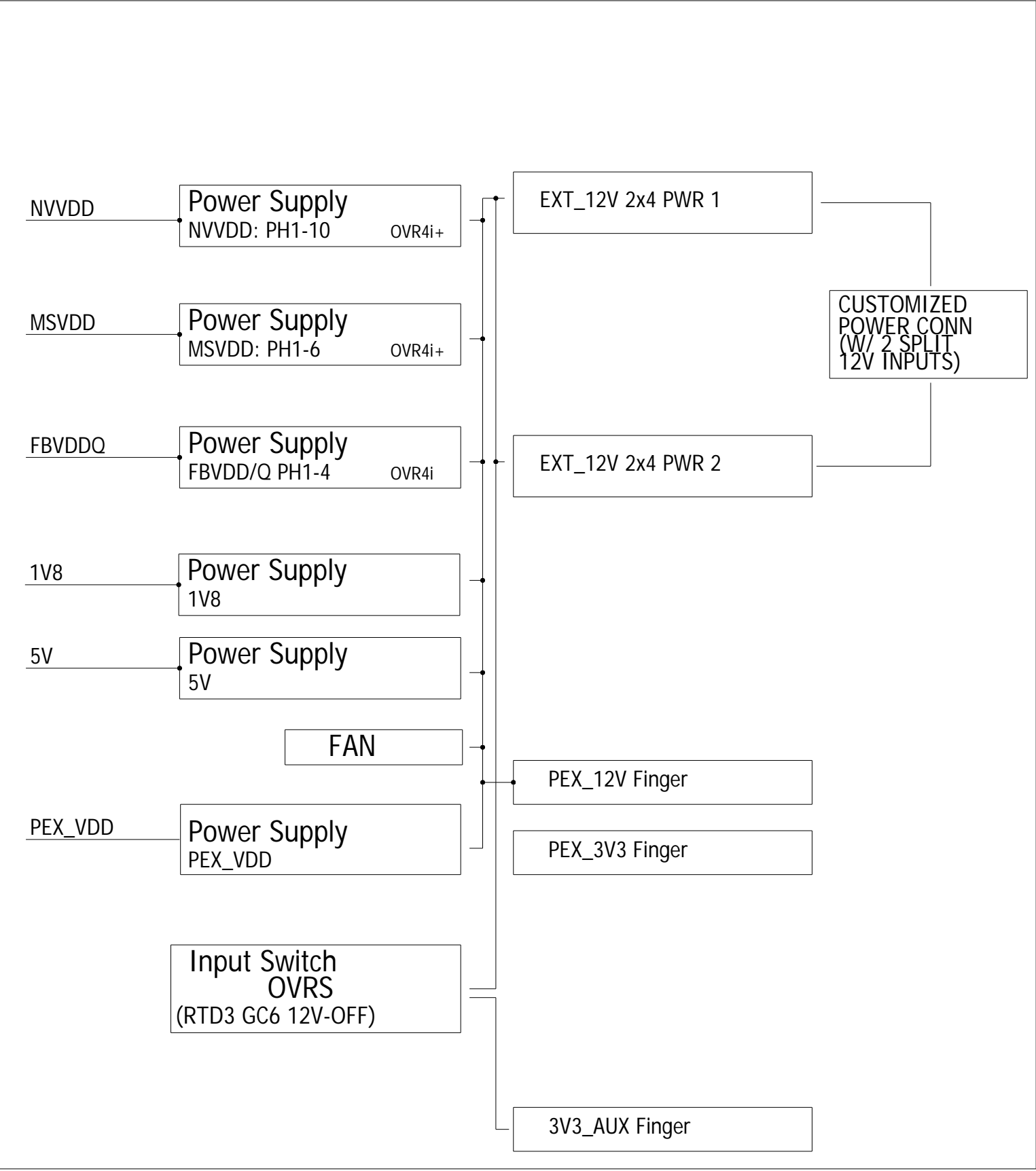
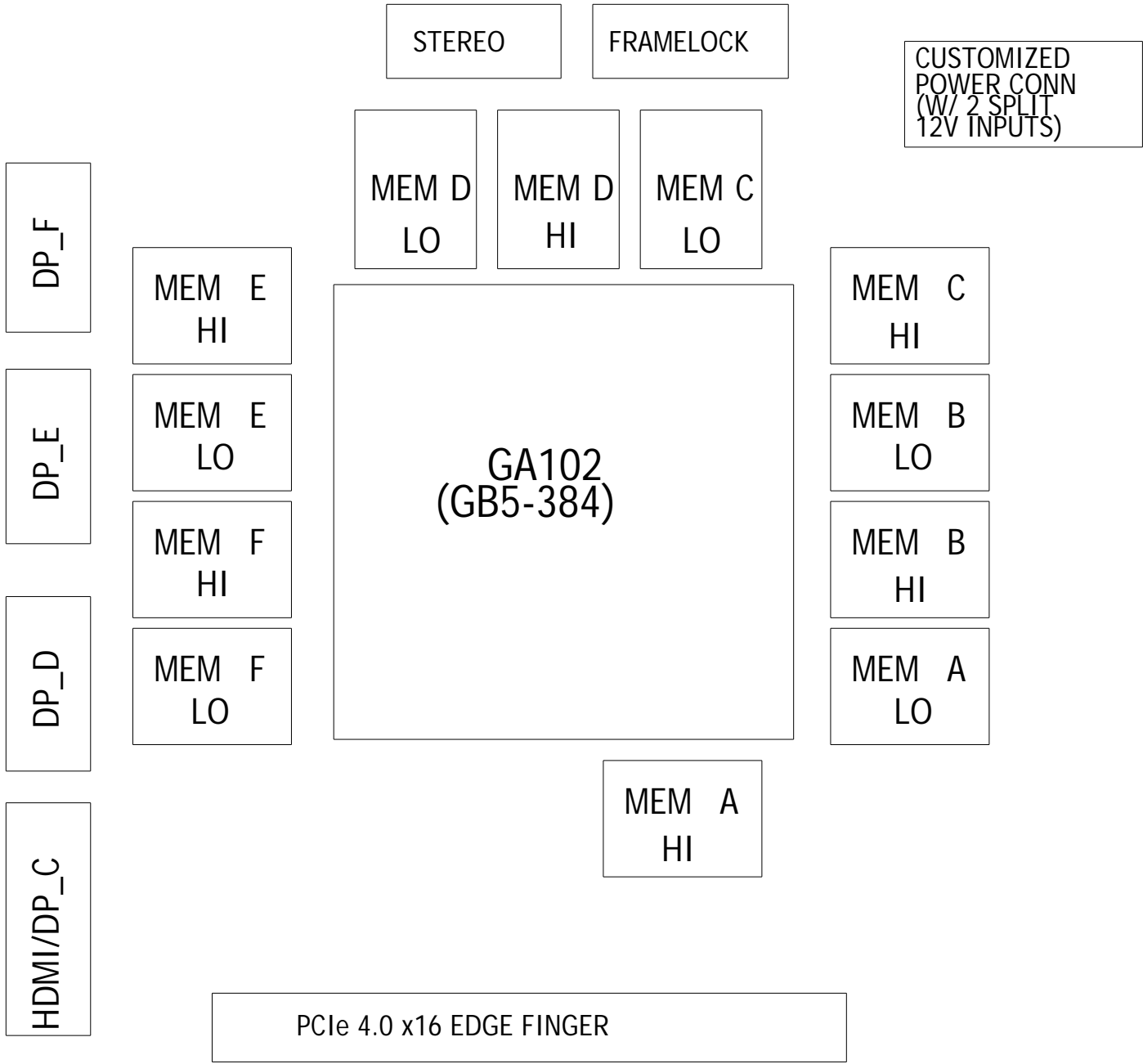
DP + DP + DP + HDMI

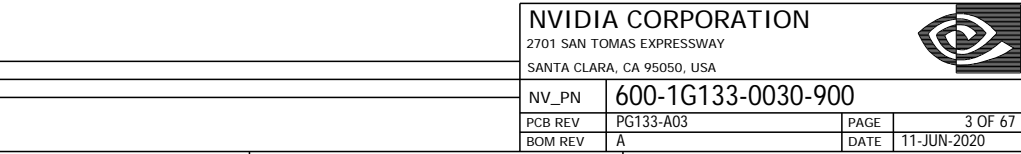
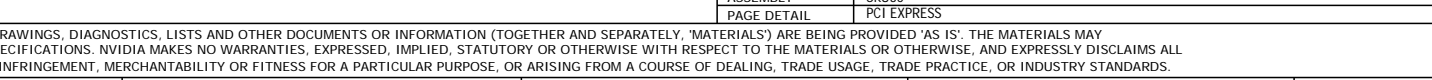
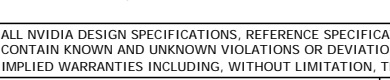
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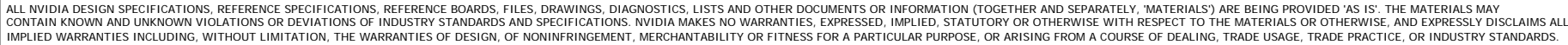
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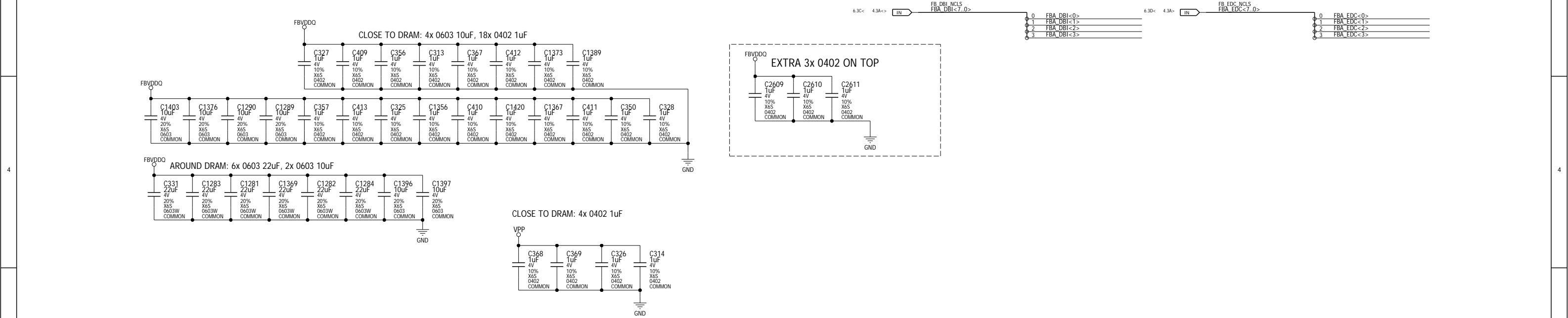
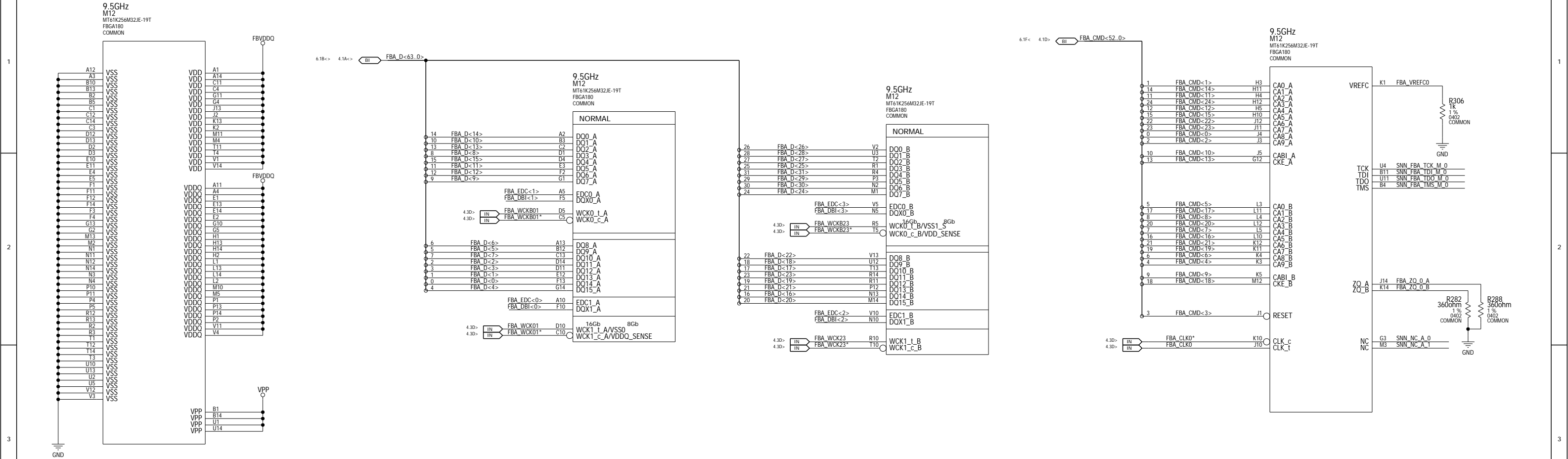
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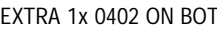
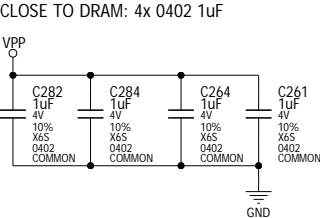
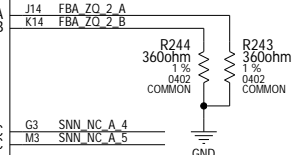
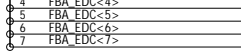
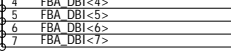
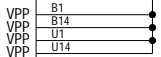
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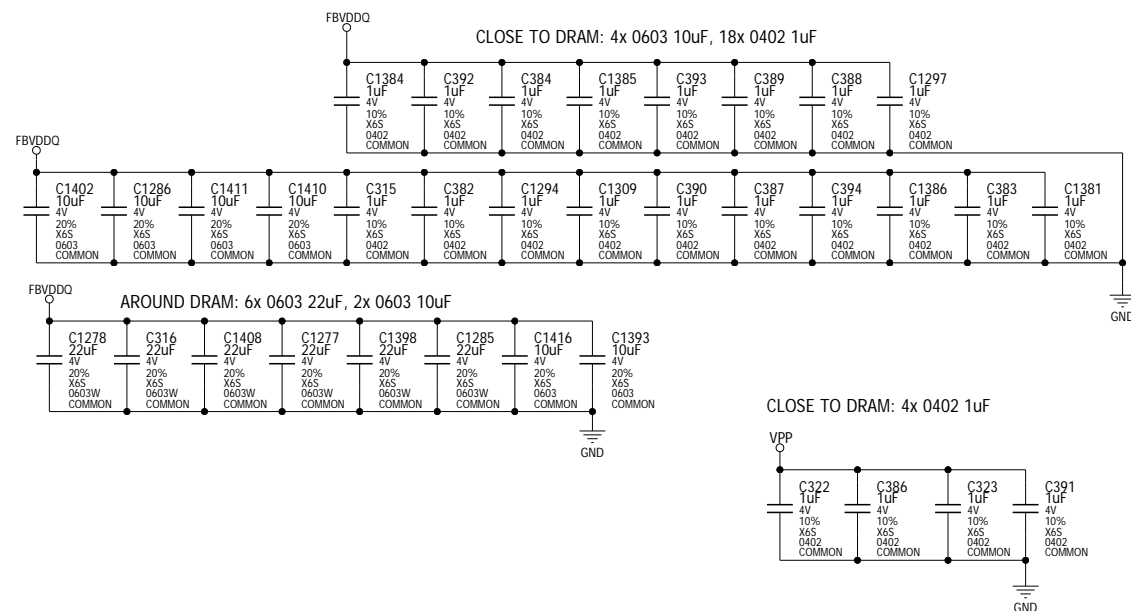
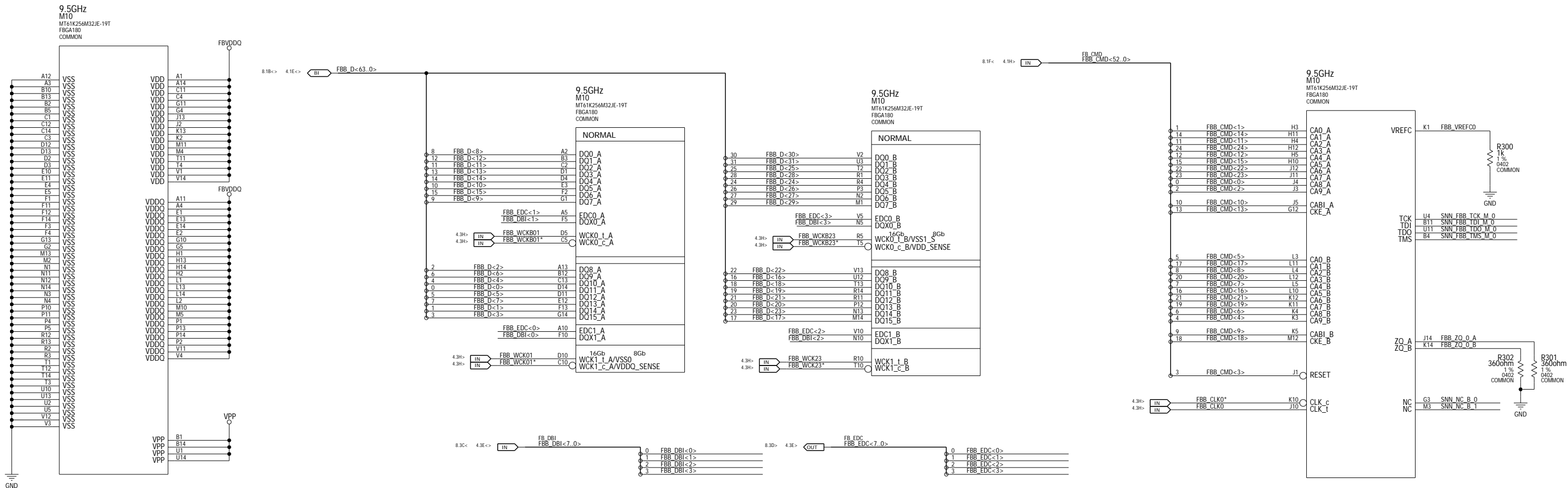









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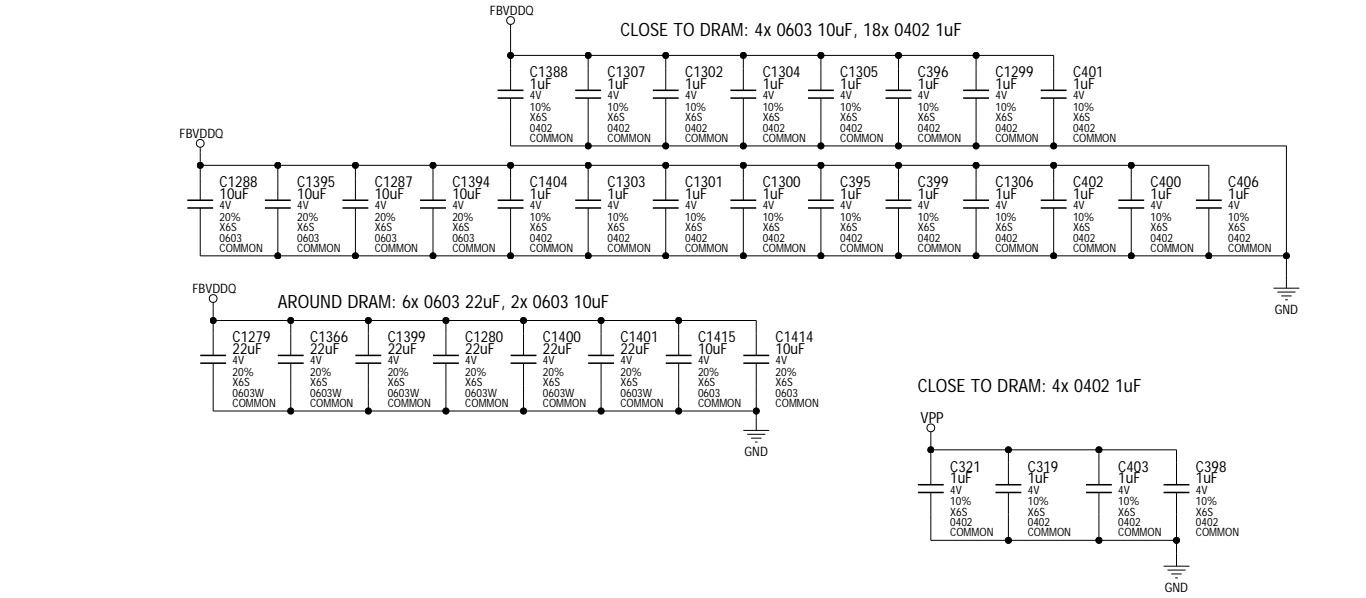
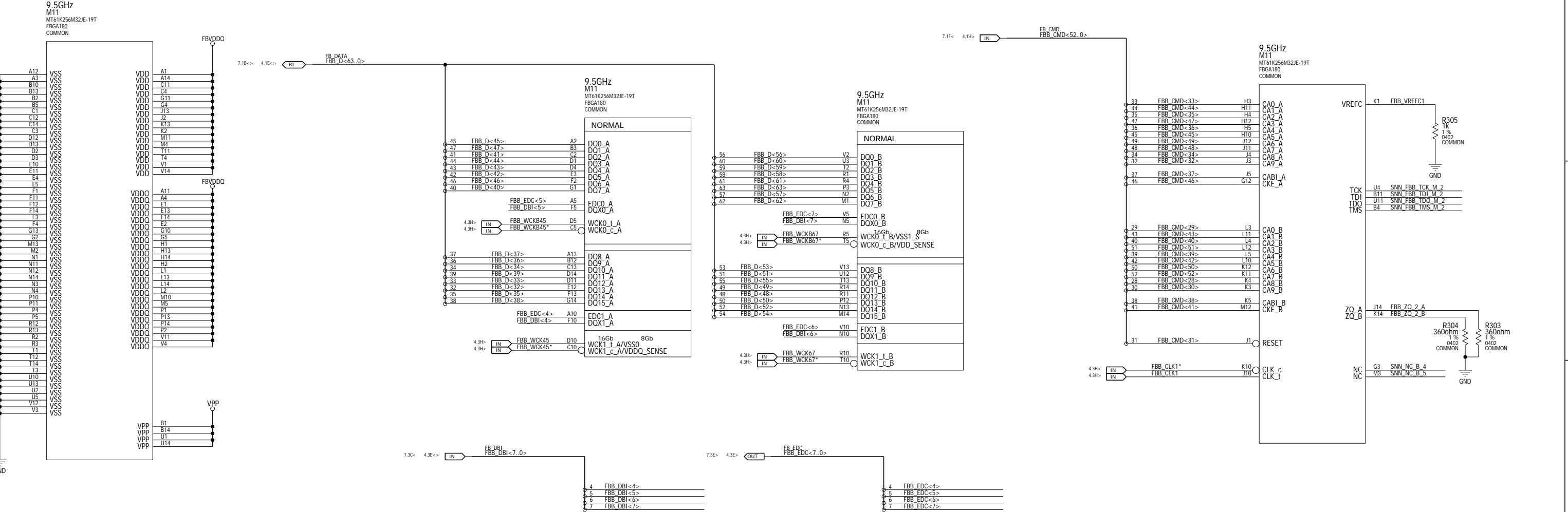


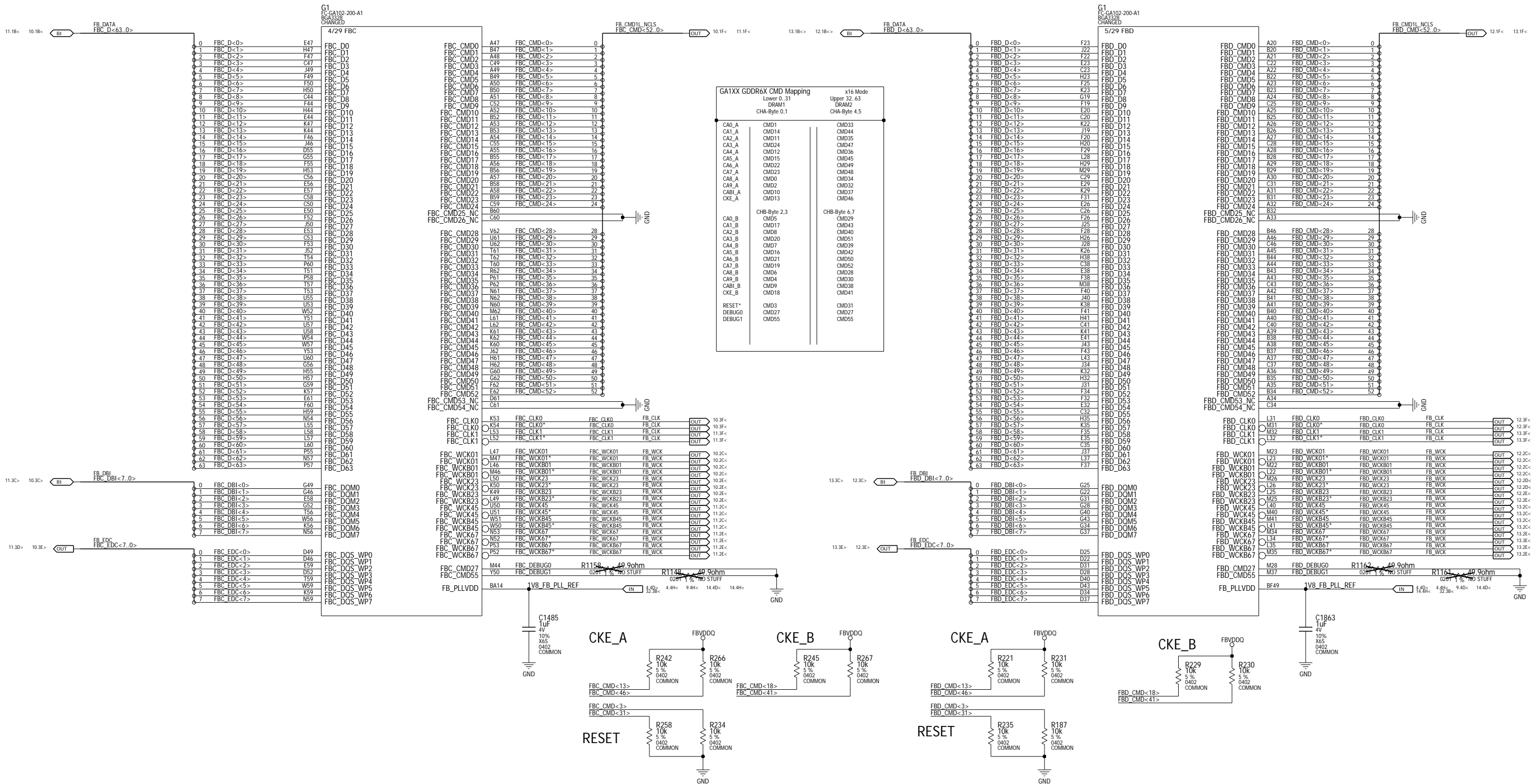
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PAGE DETAIL	MEMORY: FBB PARTITION[31:0]

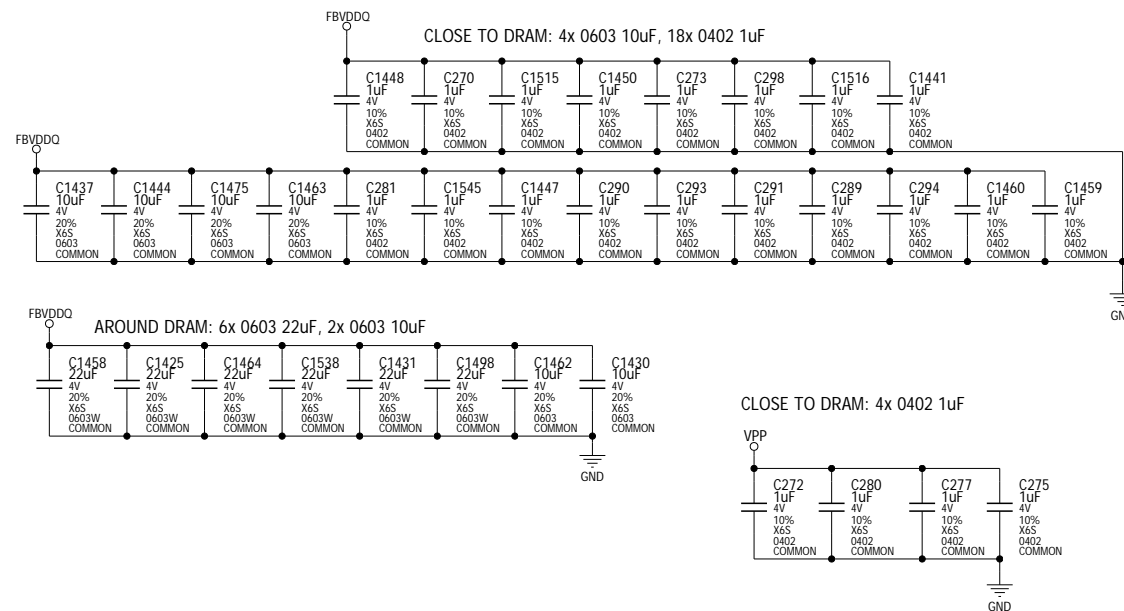
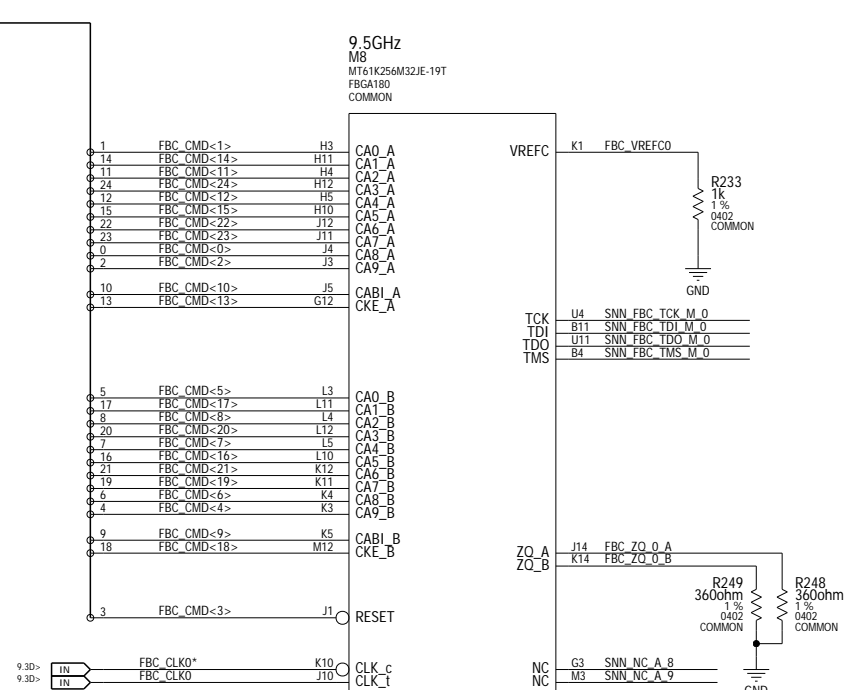
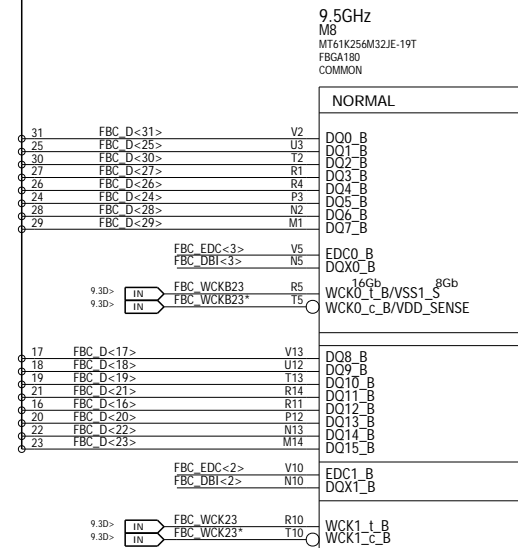
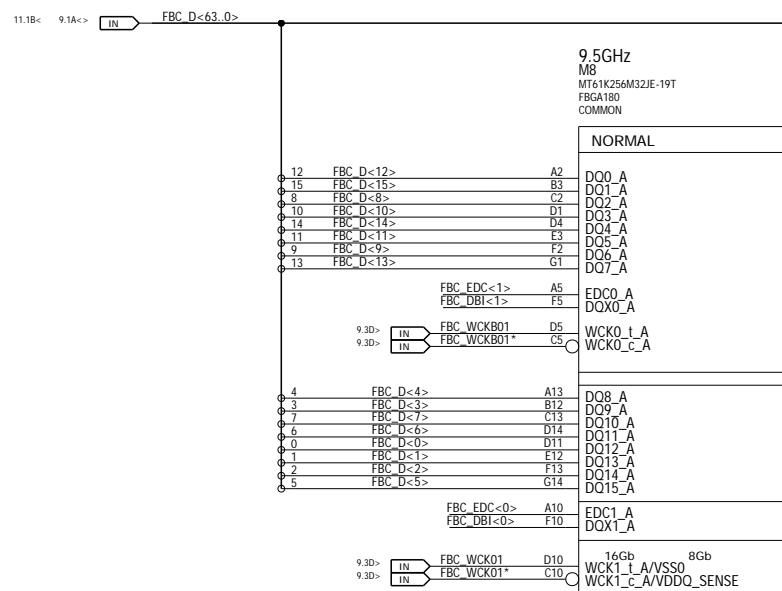
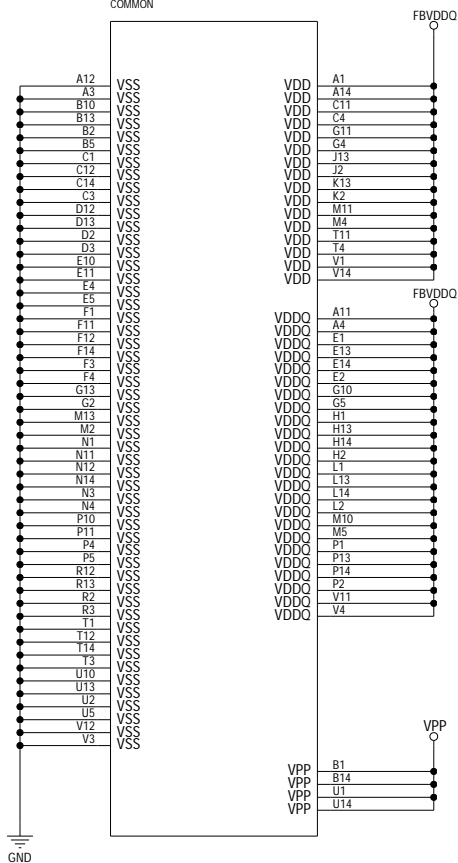
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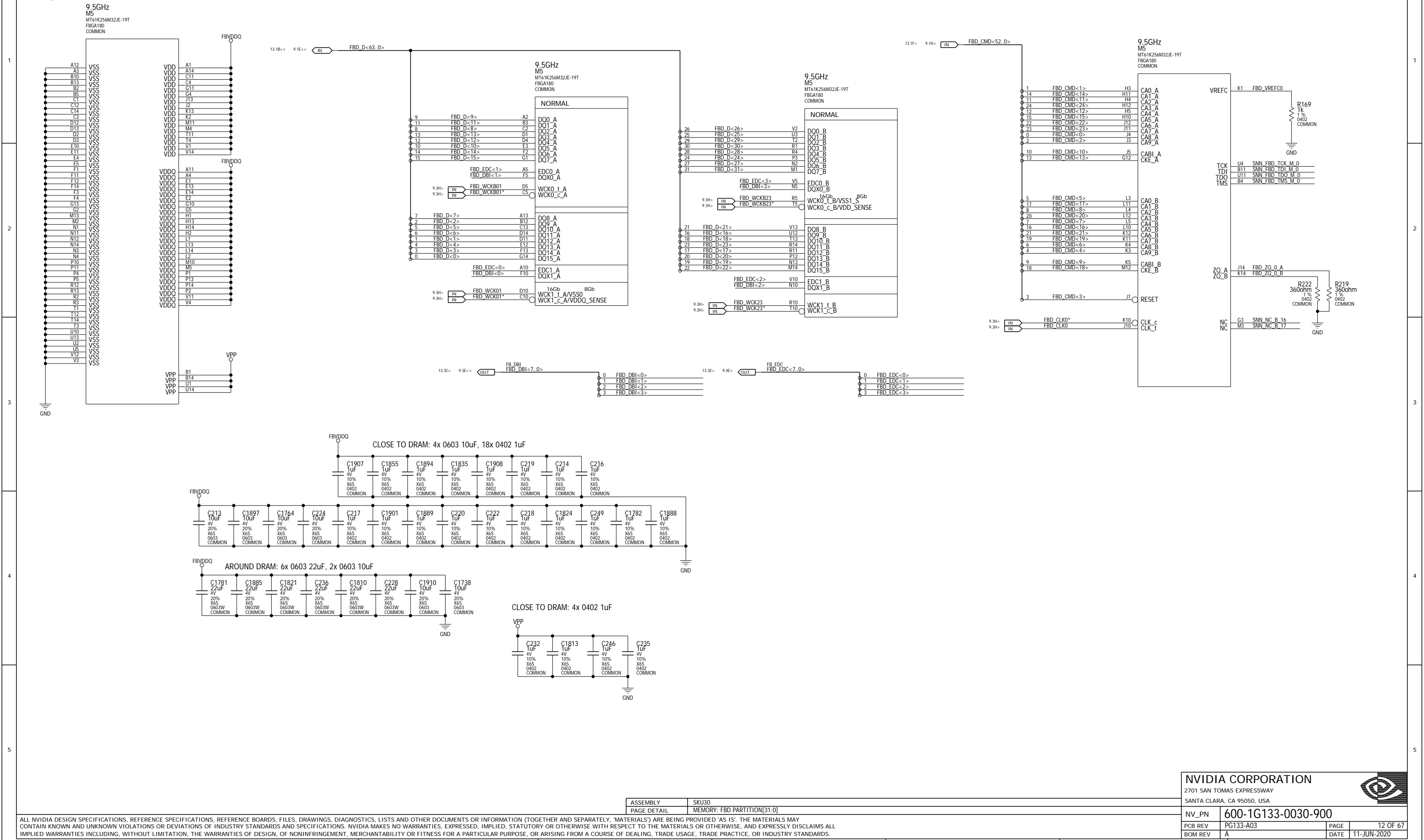


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A	B	C	D	E	F	G	H
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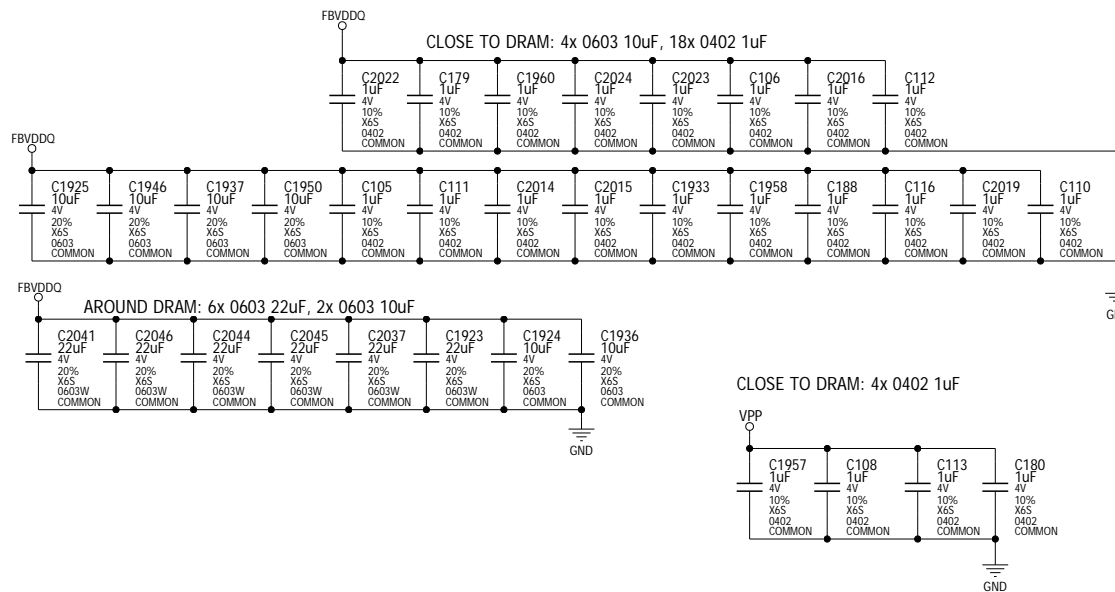
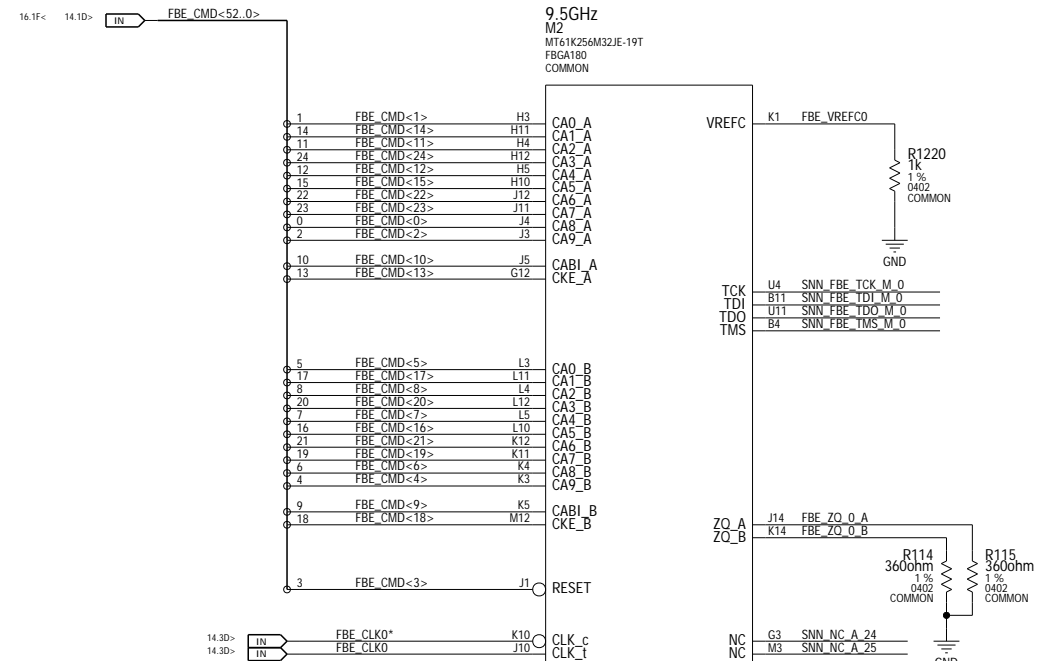
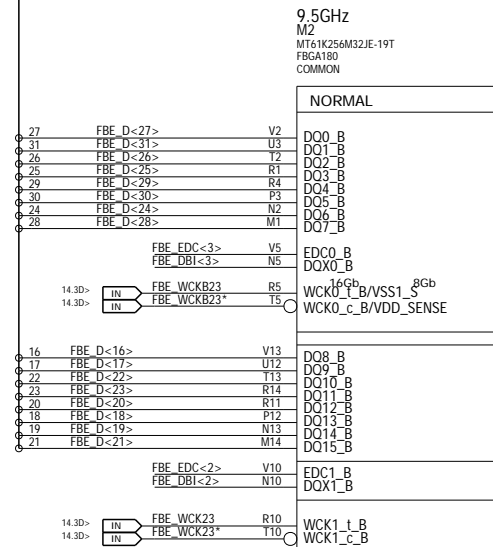
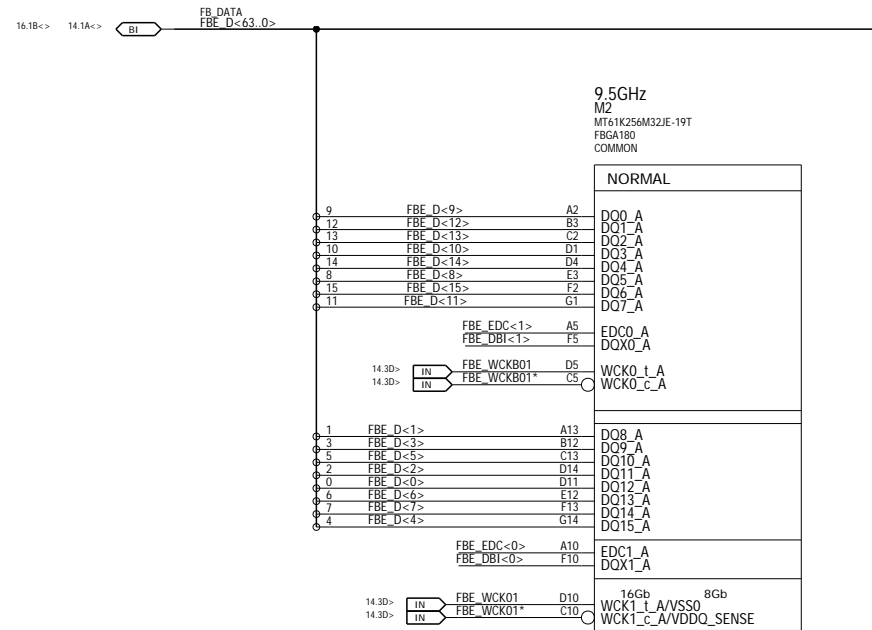
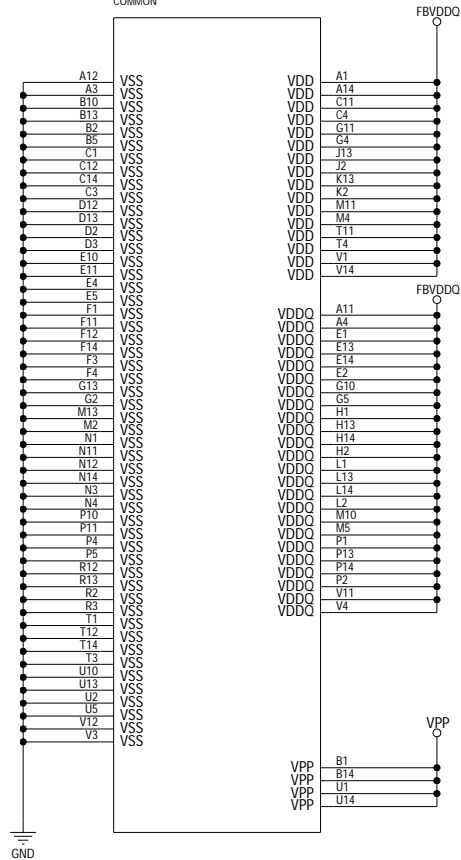
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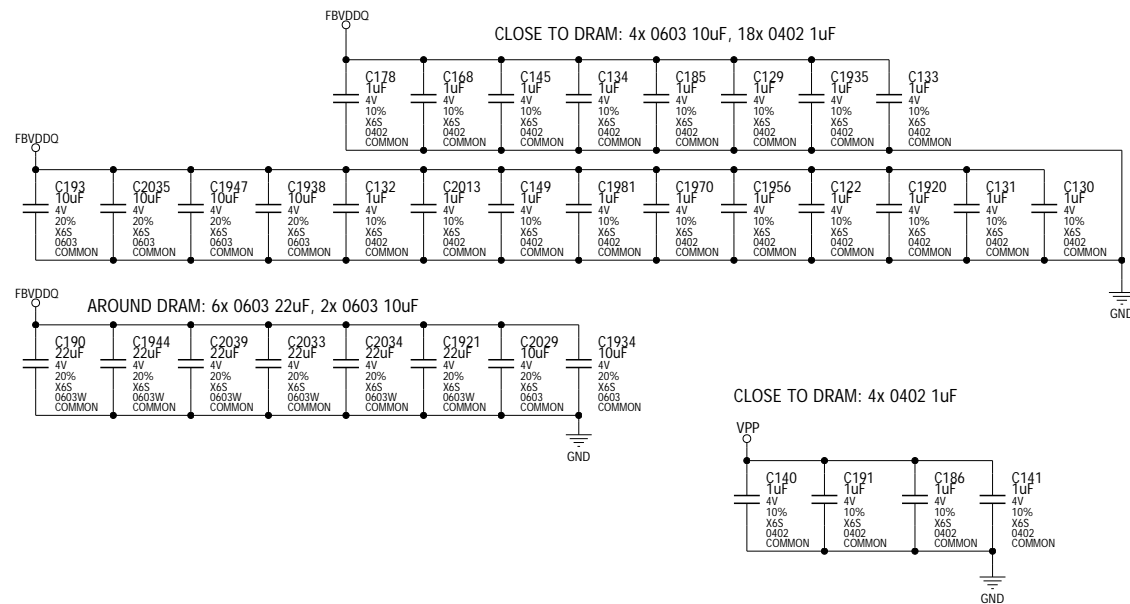
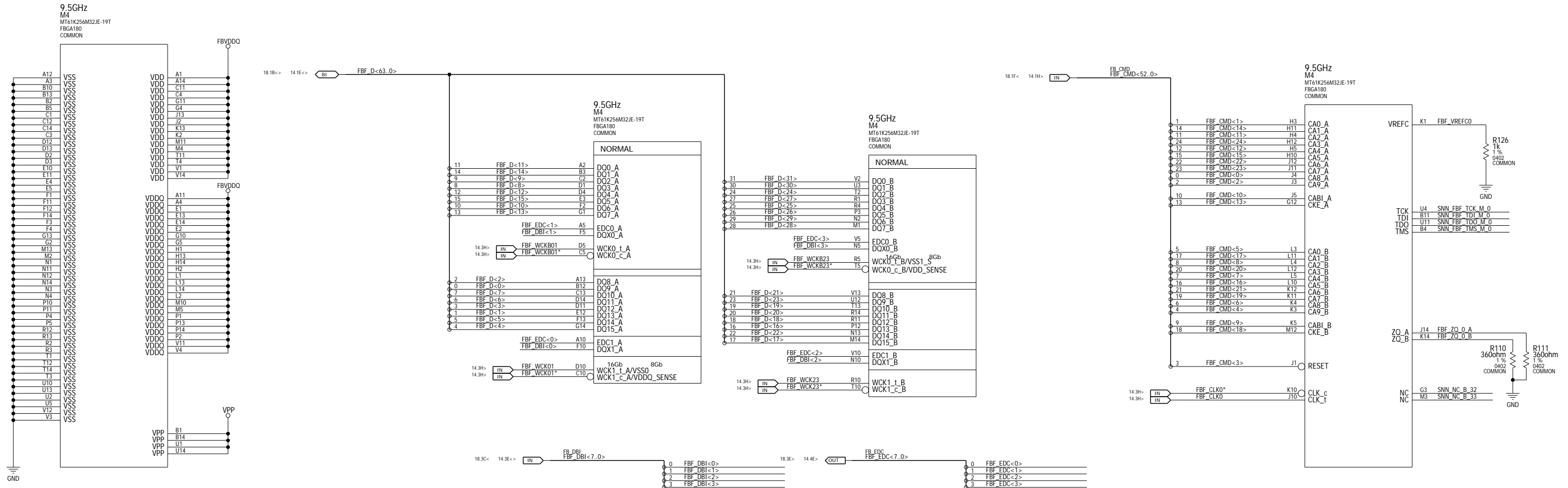
ASSEMBLY	SKU30
PAGE DETAIL	MEMORY: FBE PARTITION[31:0]

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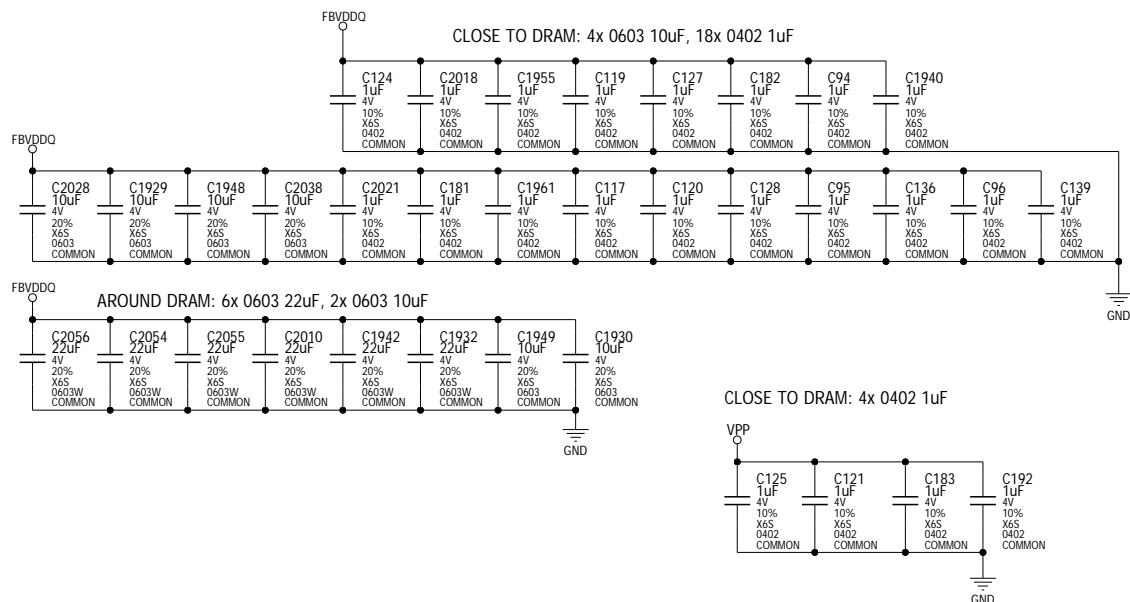
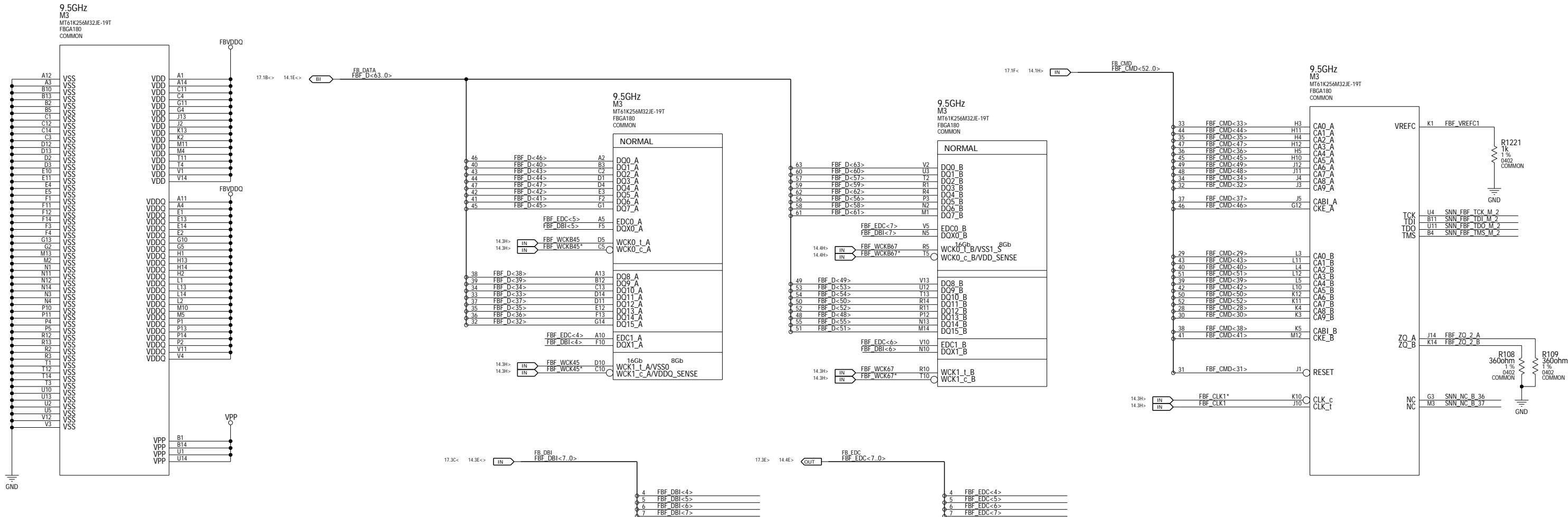


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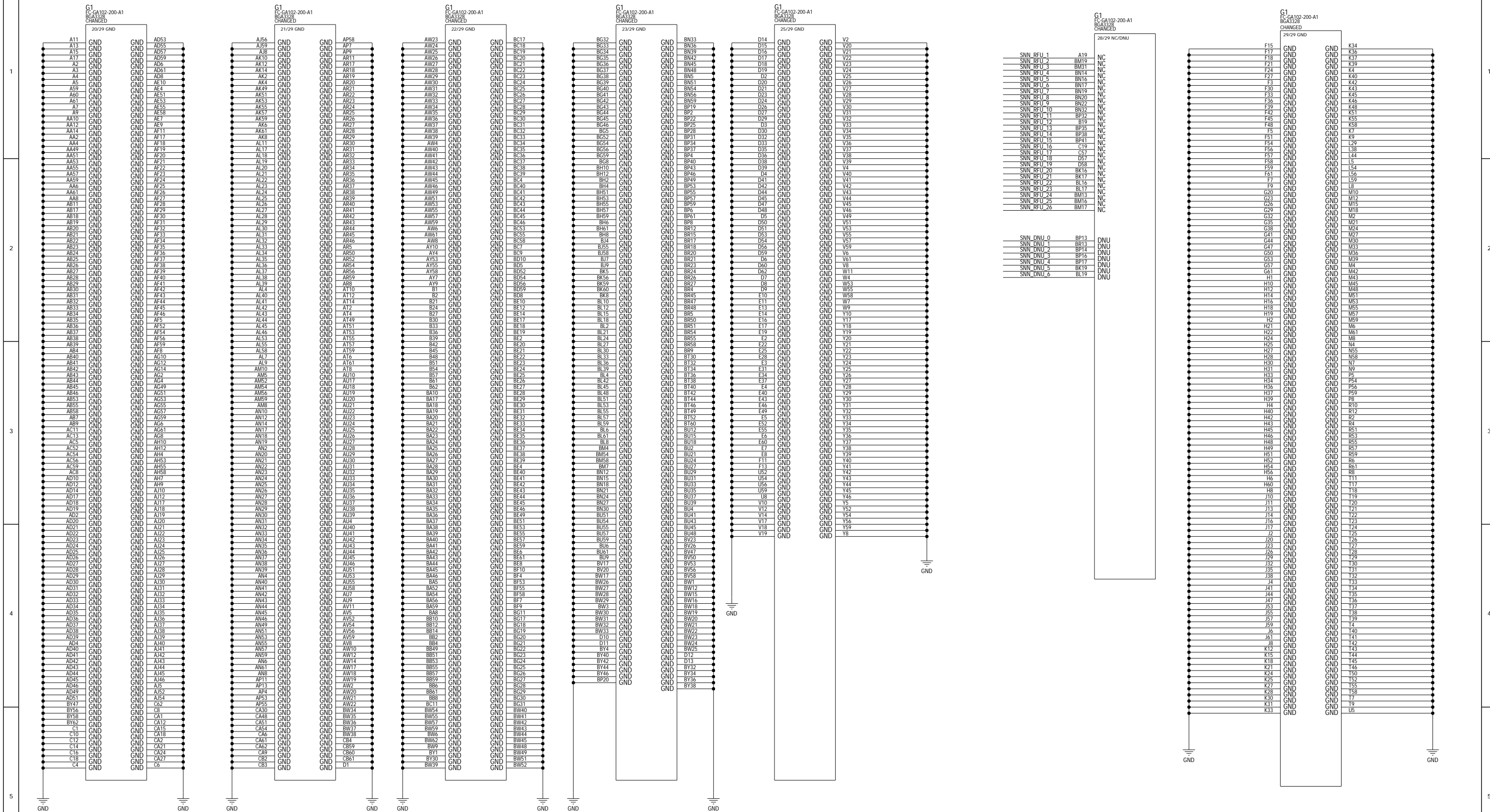
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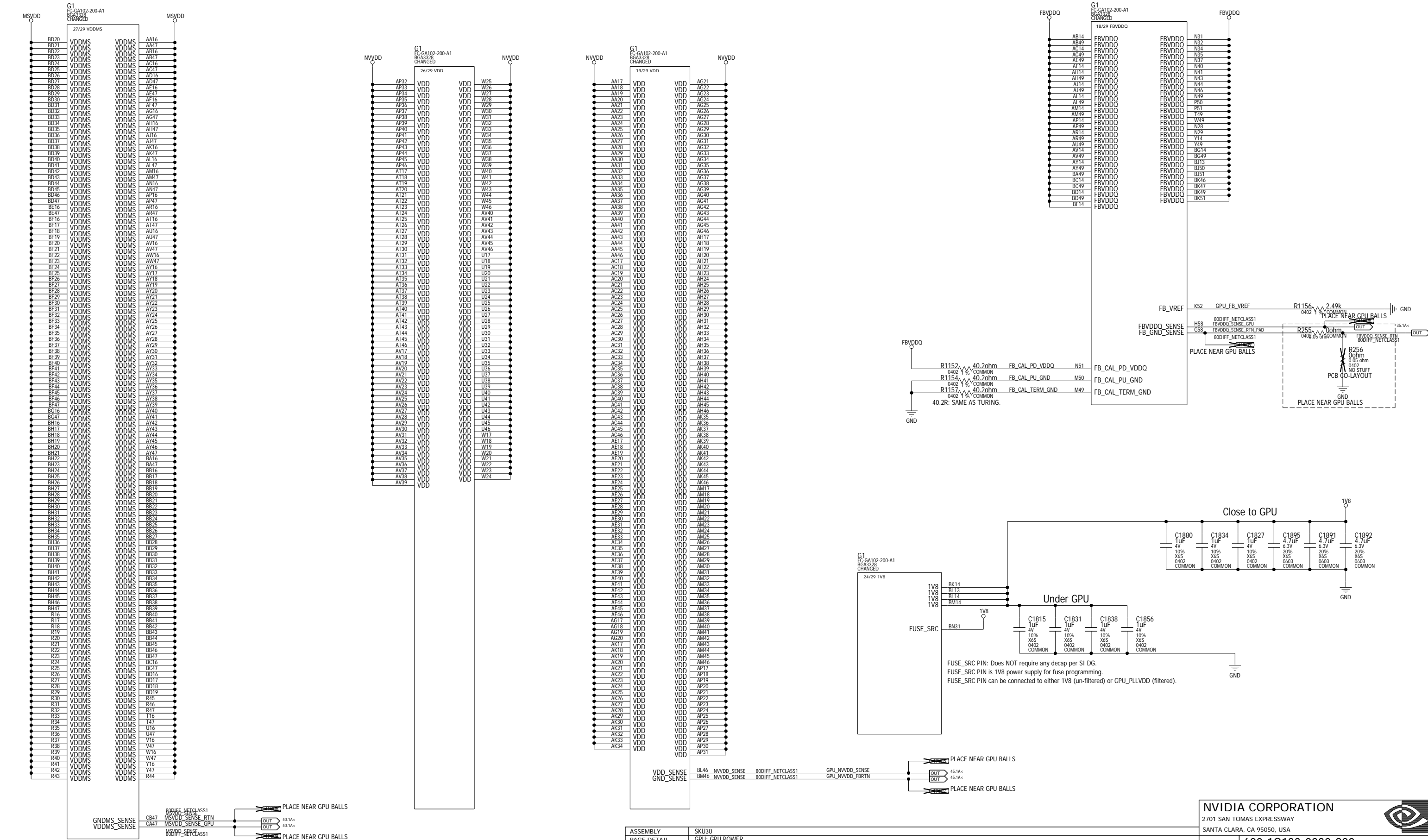


ASSEMBLY	SKU30
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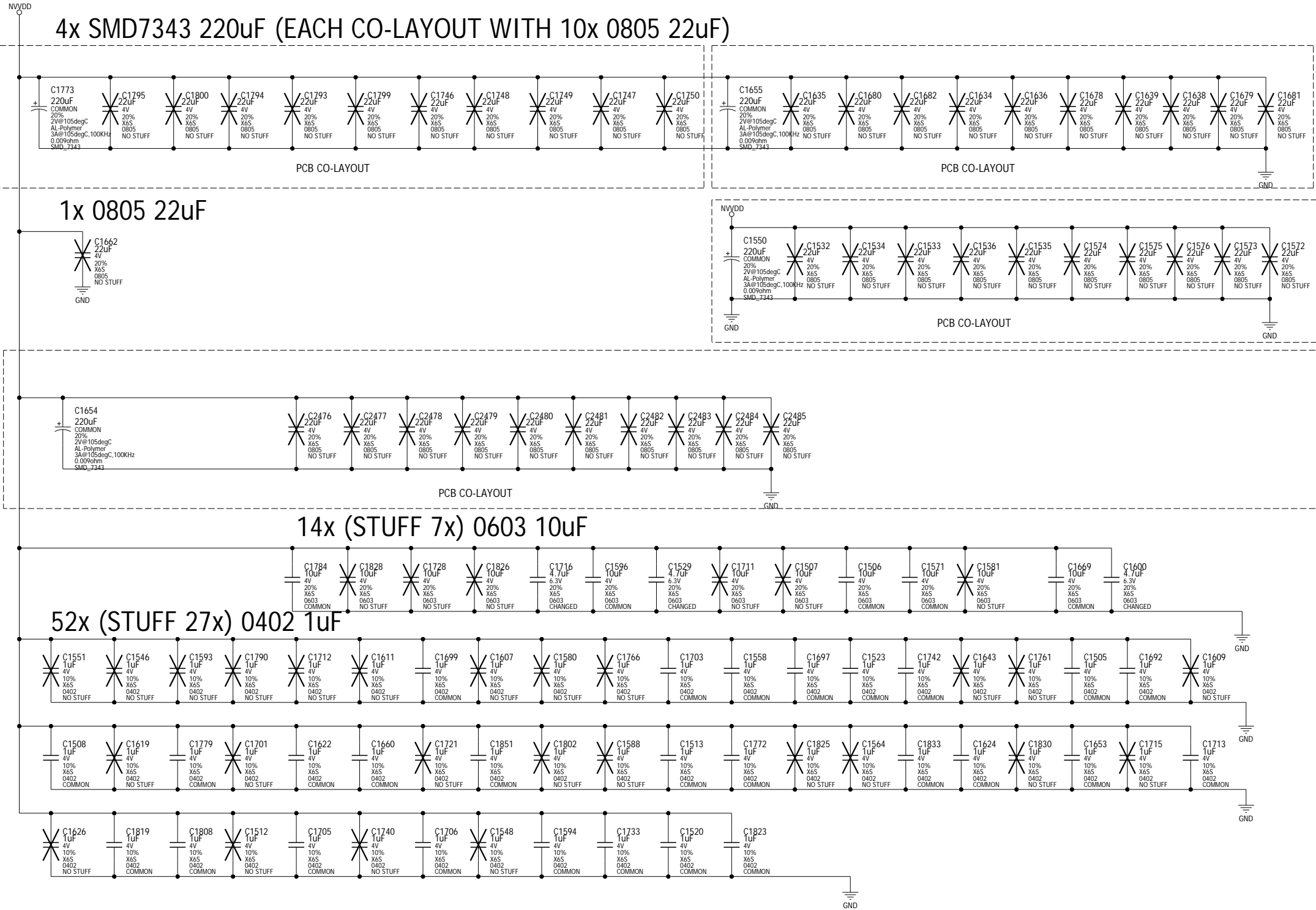
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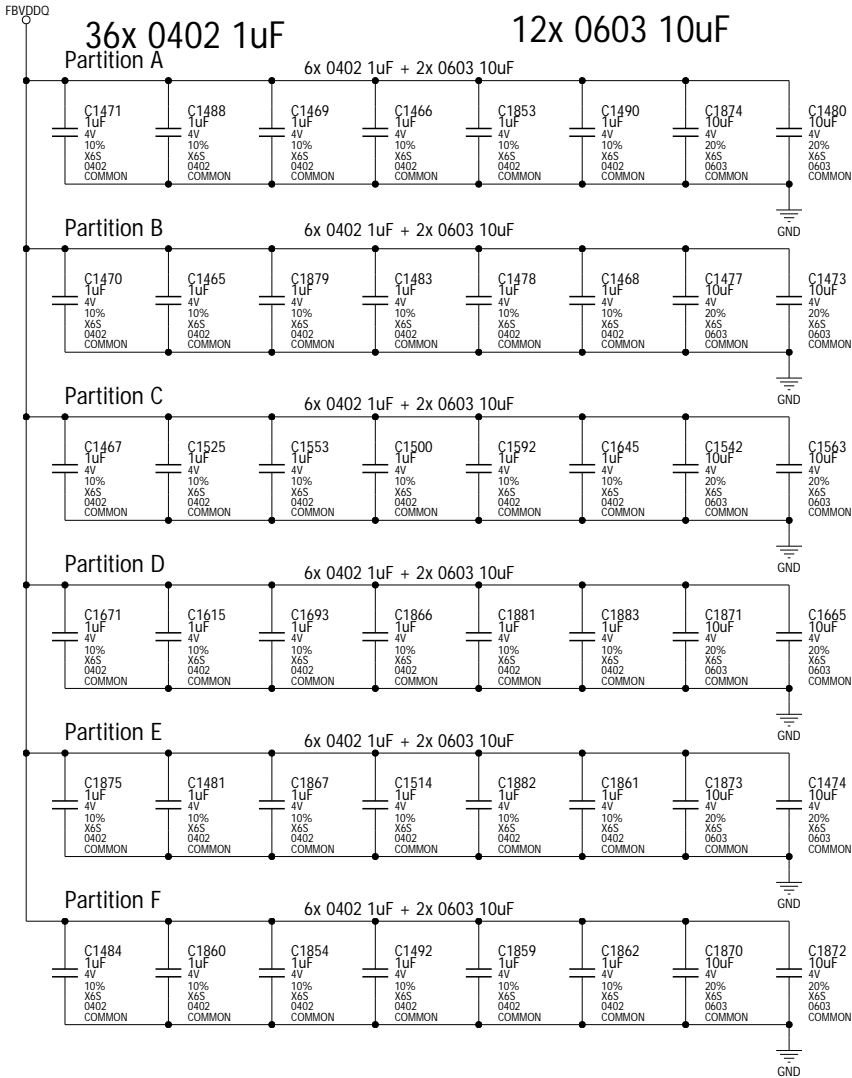


NVVDD UNDER GPU

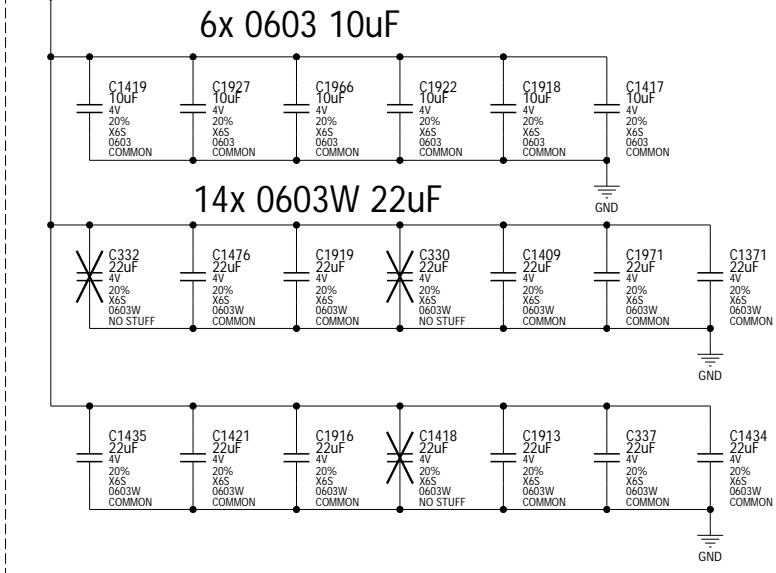


FBVDDQ

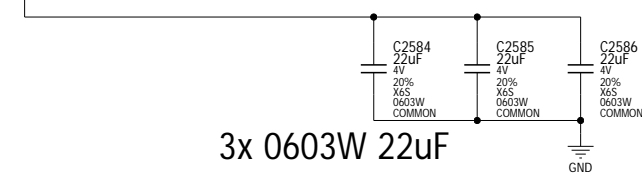
Under GPU



Close to GPU



Added for A00 x16

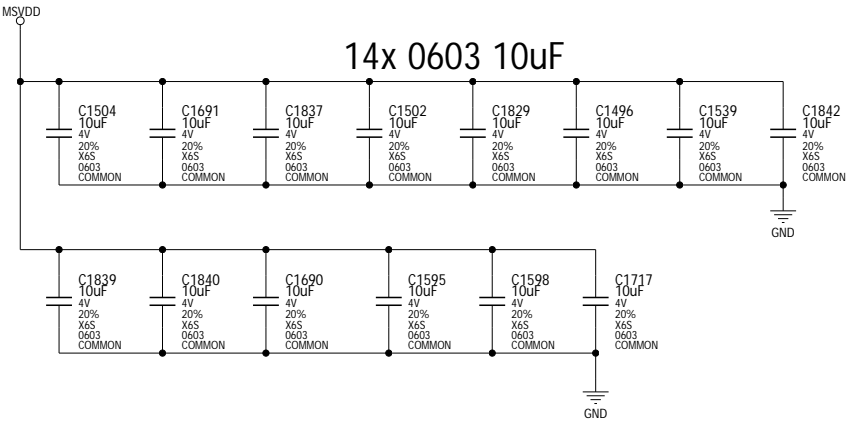


Close to GPU

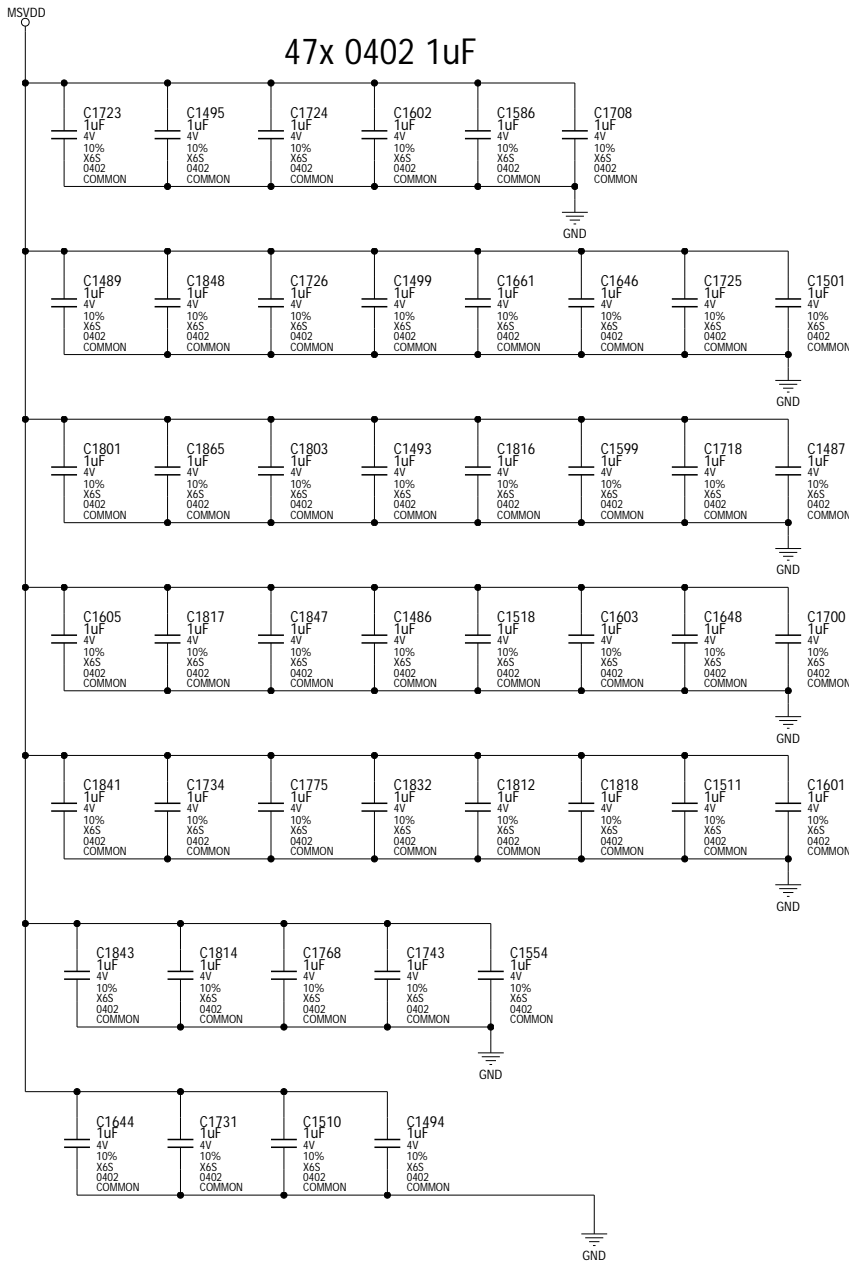
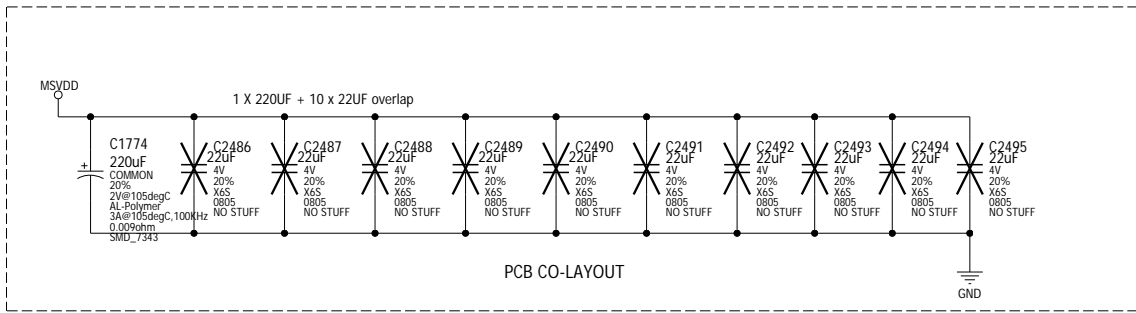
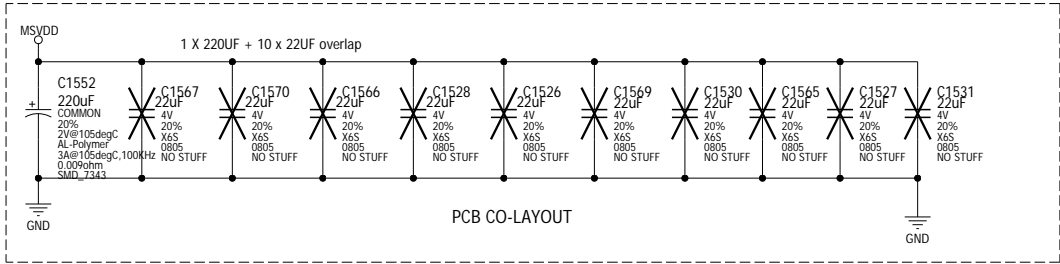
Page 23: GPU: MSVDD DECOUPLING

MSVDD

UNDER GPU

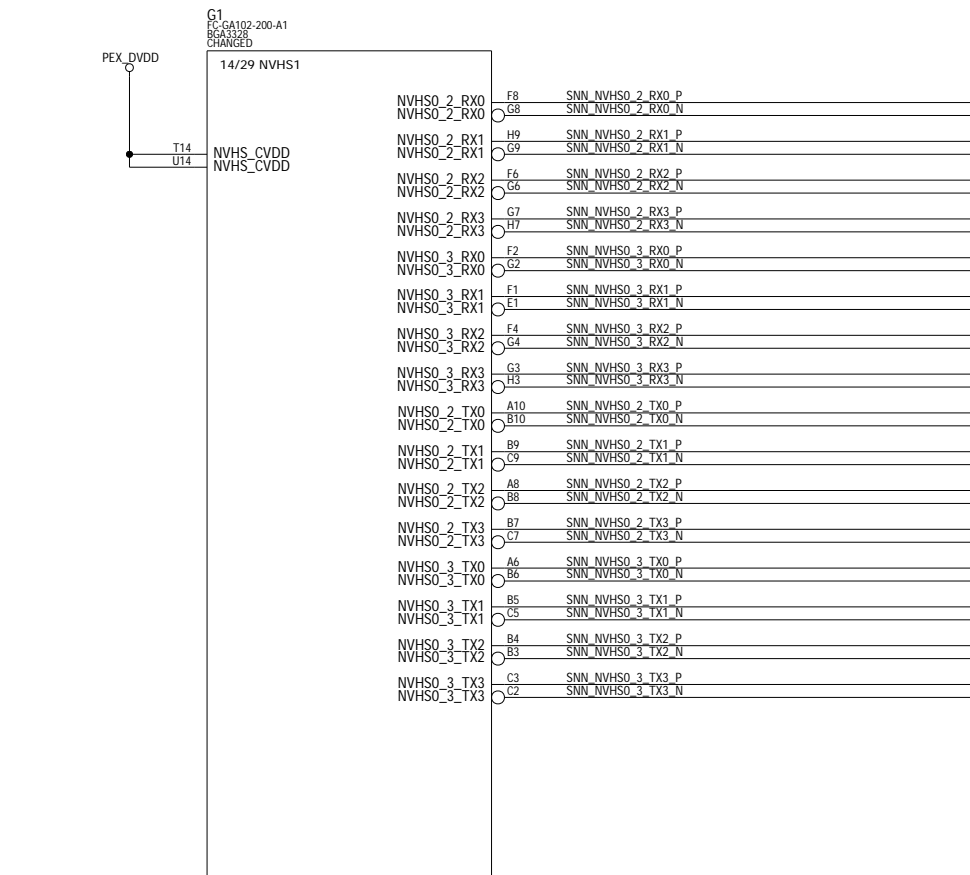
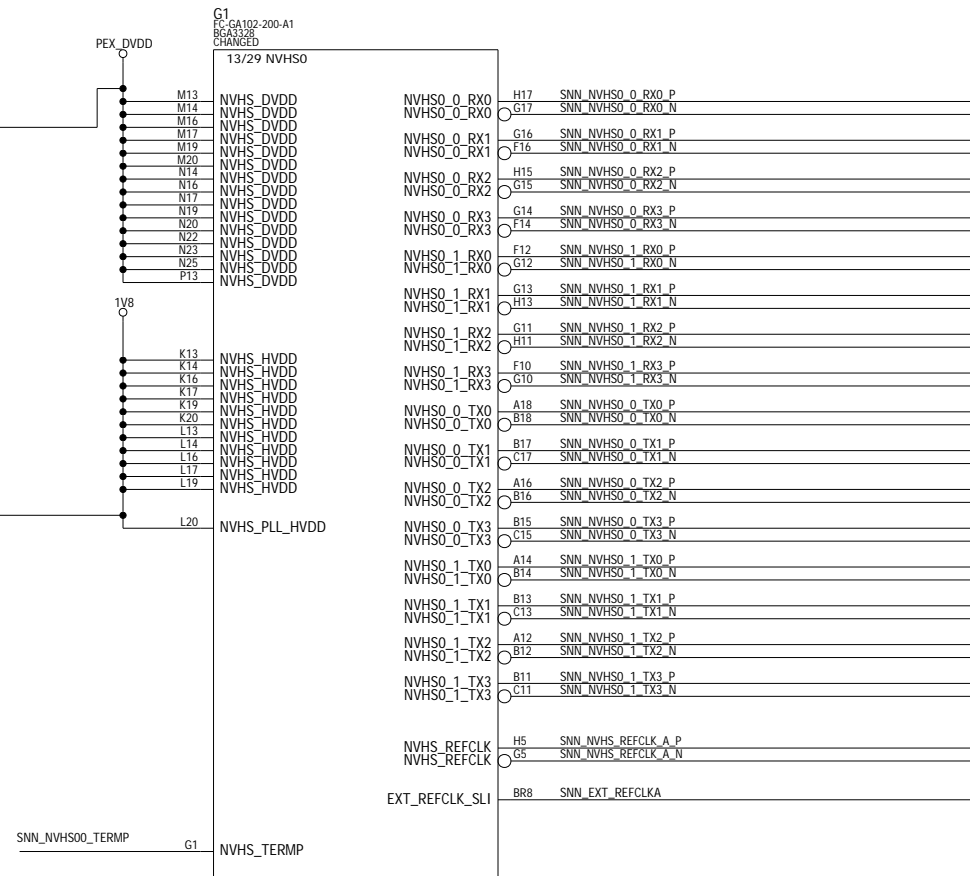
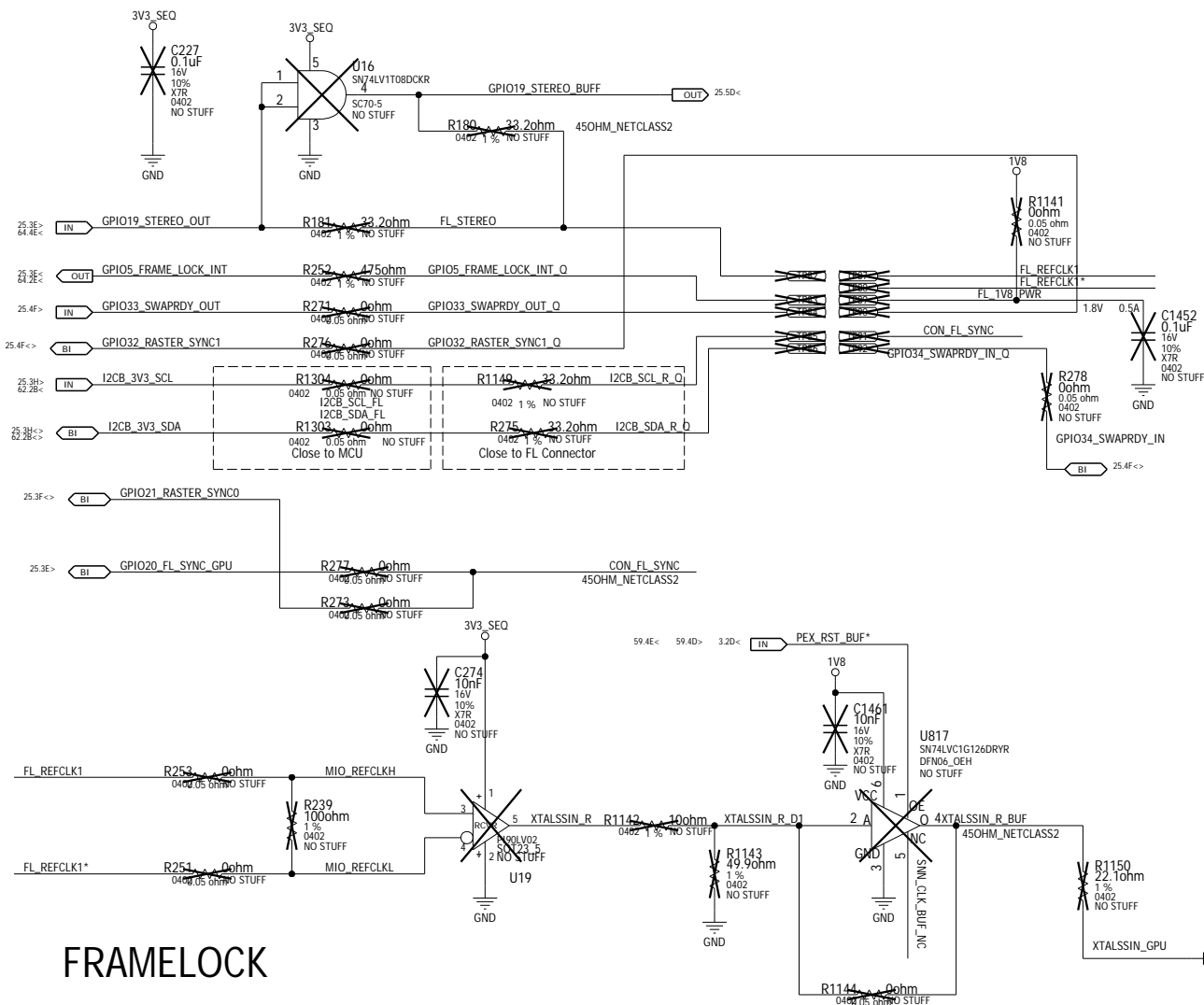
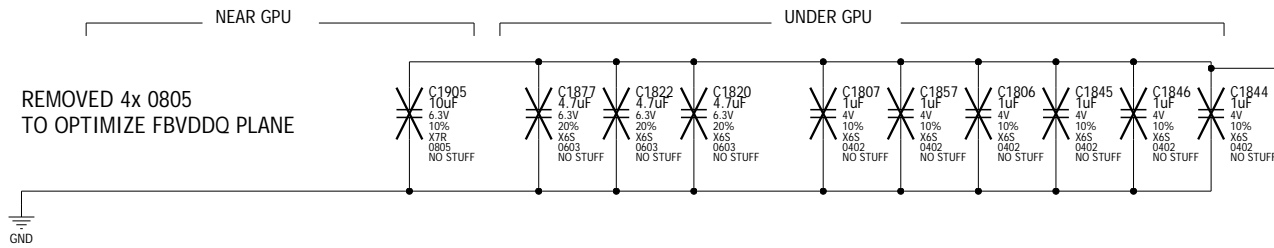
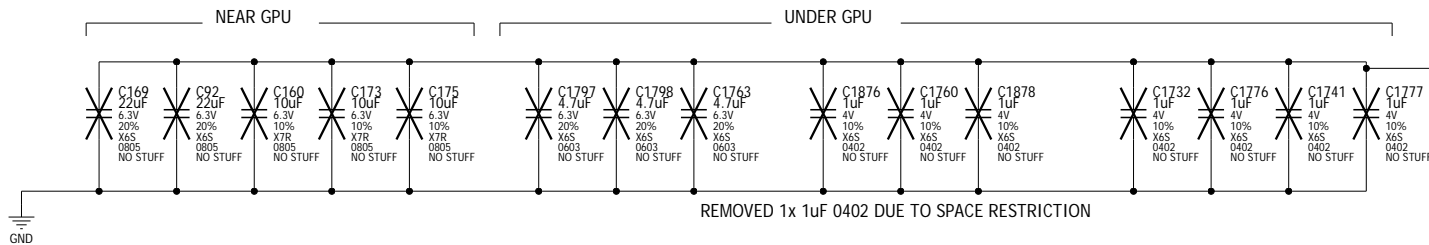


2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION






FRAMELOCK

ASSEMBLY	SKU30
PAGE DETAIL	GPU: NVHS x16, FRAMELOCK

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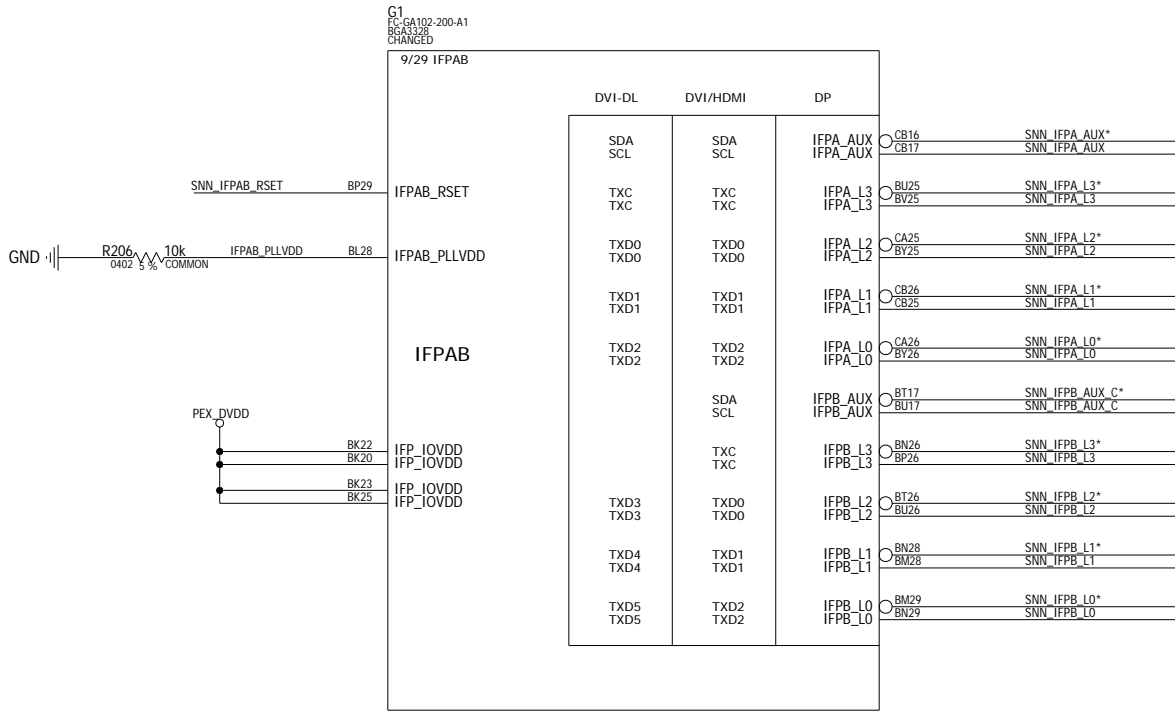
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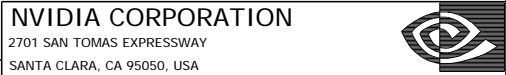
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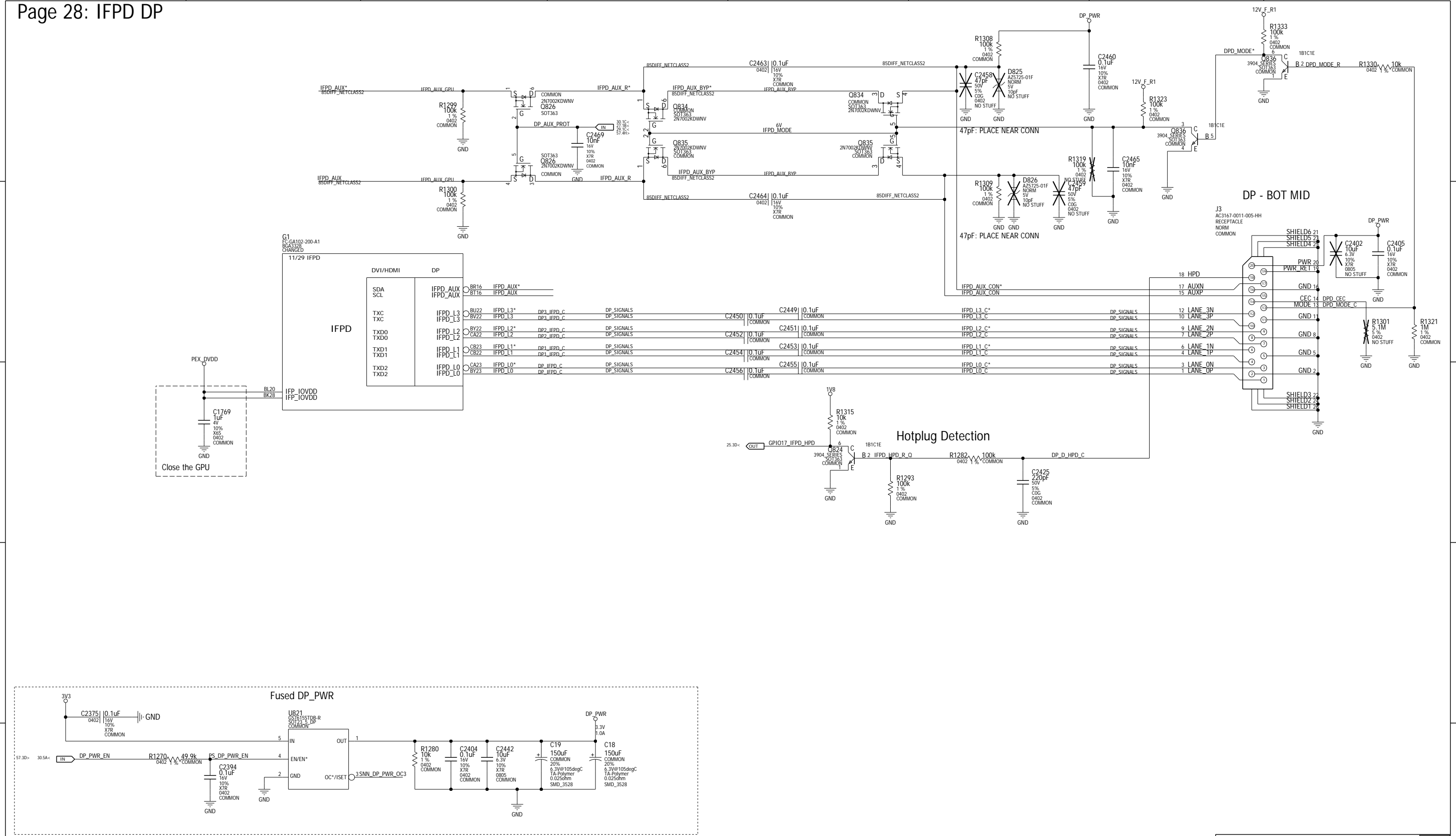
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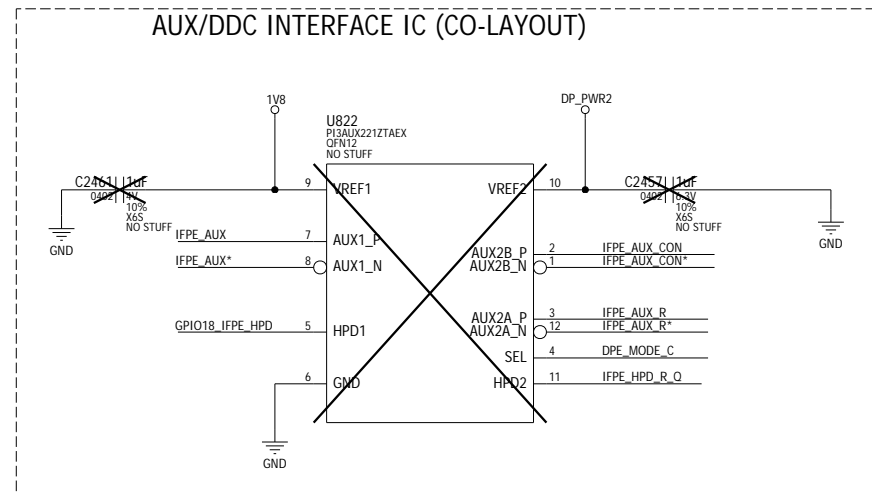
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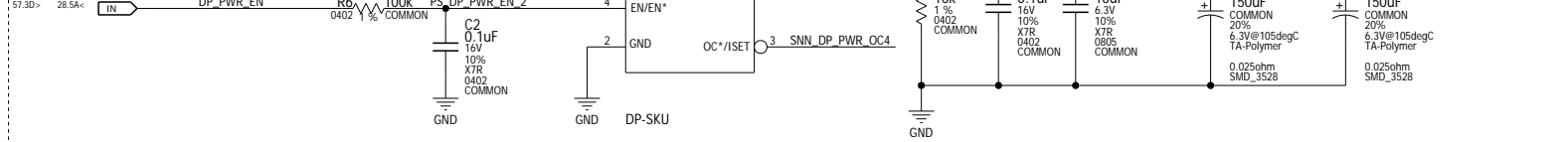
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Page 31: MISC: ROM, Straps

GROUP0 STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)
H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)
L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)
L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)
M	H	L	01110	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)

GROUP1 ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	M	L	1001	FAN0/1=33%/33%, FS_OVERT ENABLE
H	H	H	0111	FAN0/1=66%/66%, FS_OVERT ENABLE

GROUP2 STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

<-DEFAULT

- 1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL
- 1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

<-Default

STRAP0	CA7	STRAP0
STRAP1	CB7	STRAP1
STRAP2	BW8	STRAP2
STRAP3	BW7	STRAP3
STRAP4	BY7	STRAP4
STRAP5	BV8	STRAP5

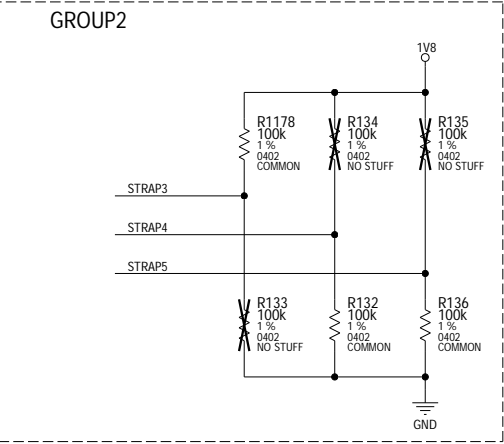
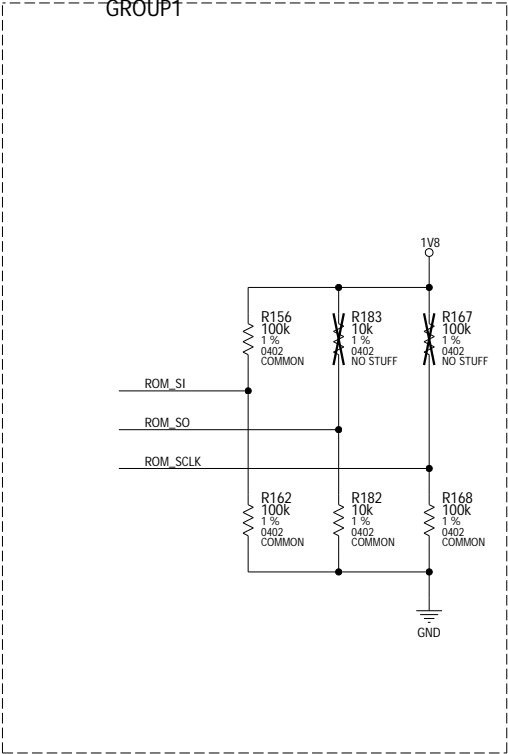
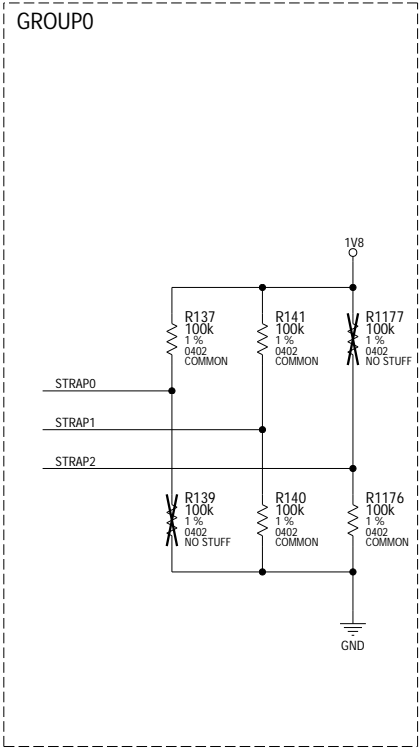
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

<-A01 PCB

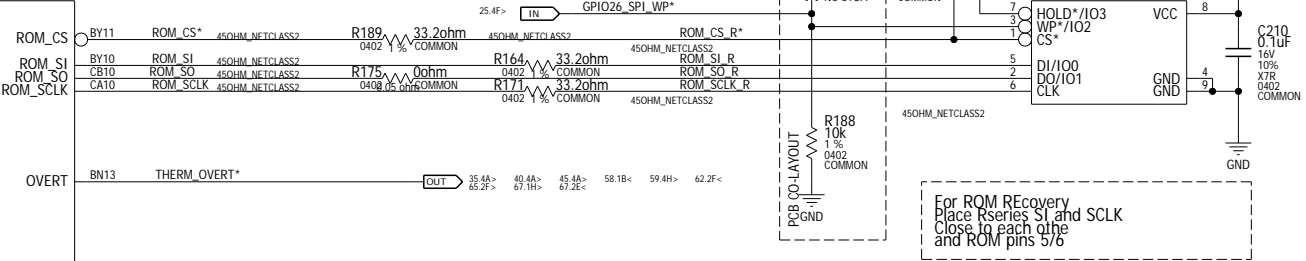
<-OLD

<-DISMISSED

<-LATEST A02/A03 PCB



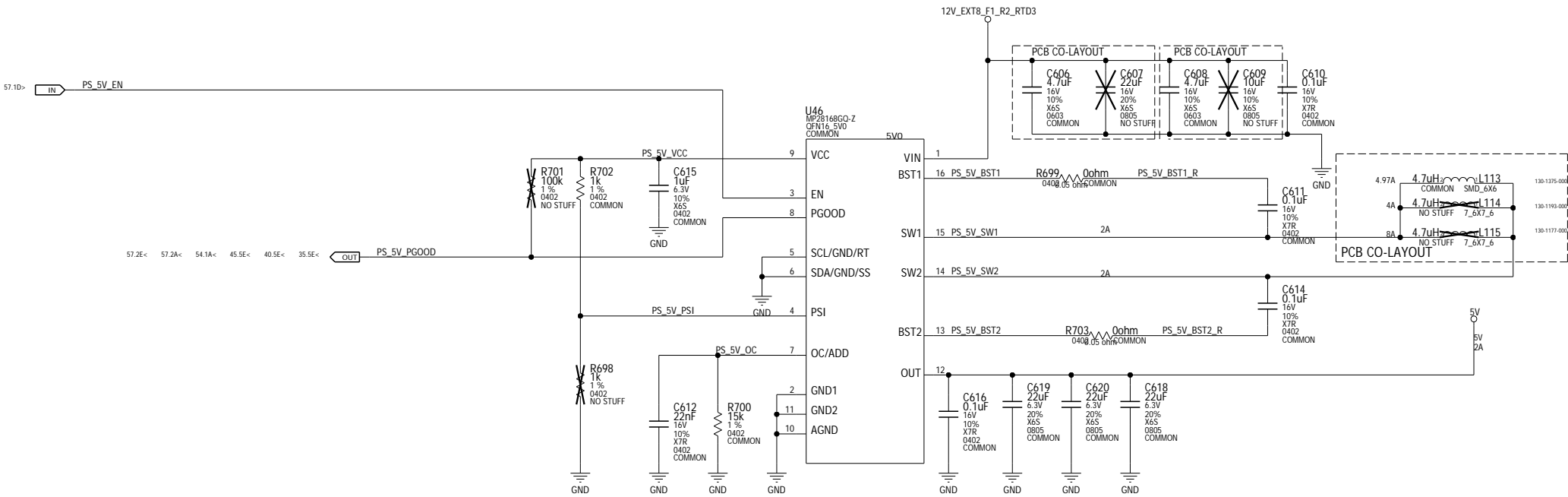
G1
FC:GA102-200-A1
BGA3328
CHANGED



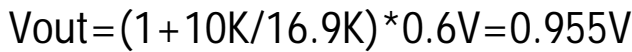
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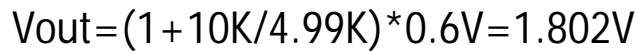
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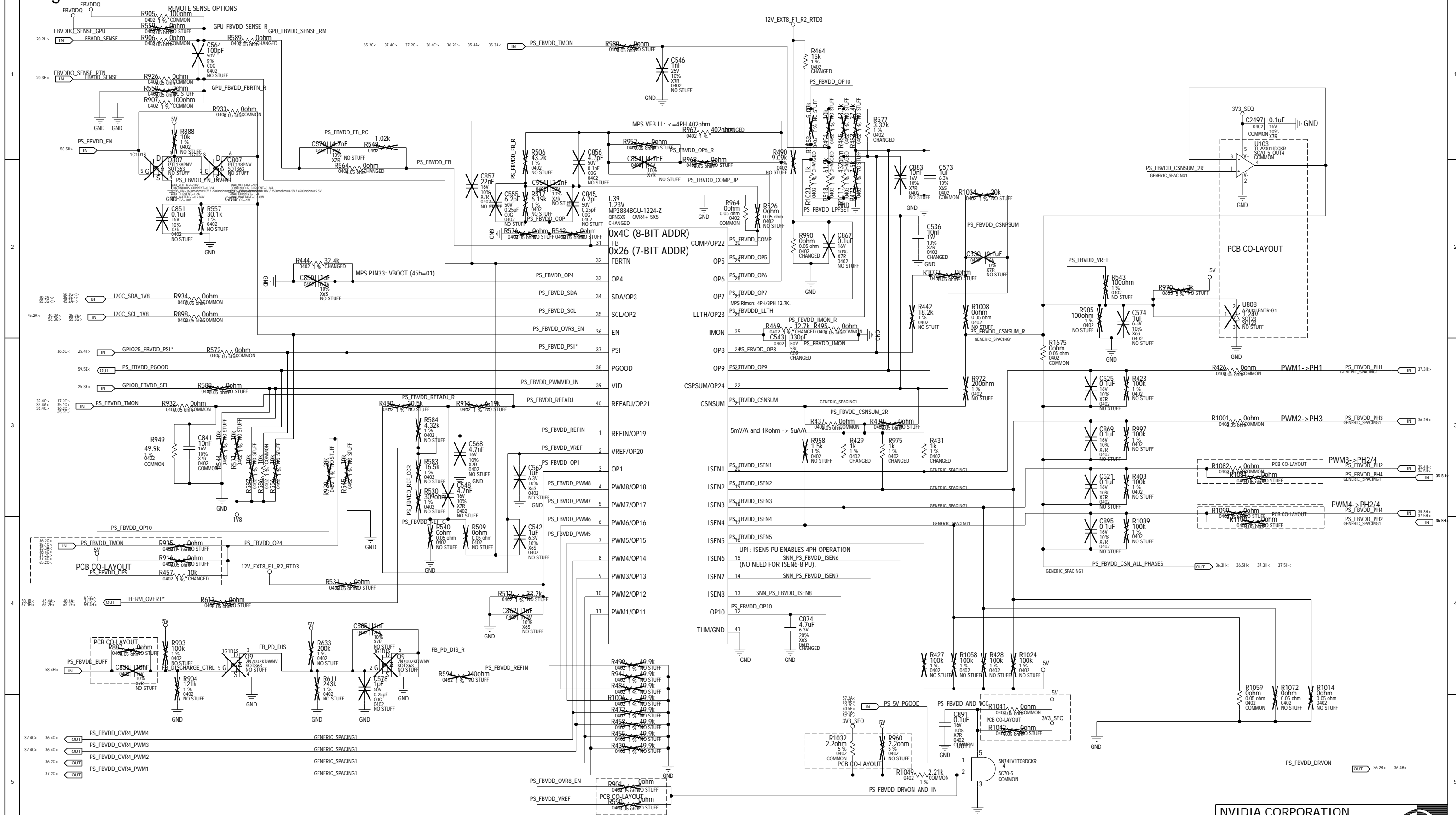
1V8



NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
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Page 35: PS: FBVDD Controller



NVIDIA CORPORATION

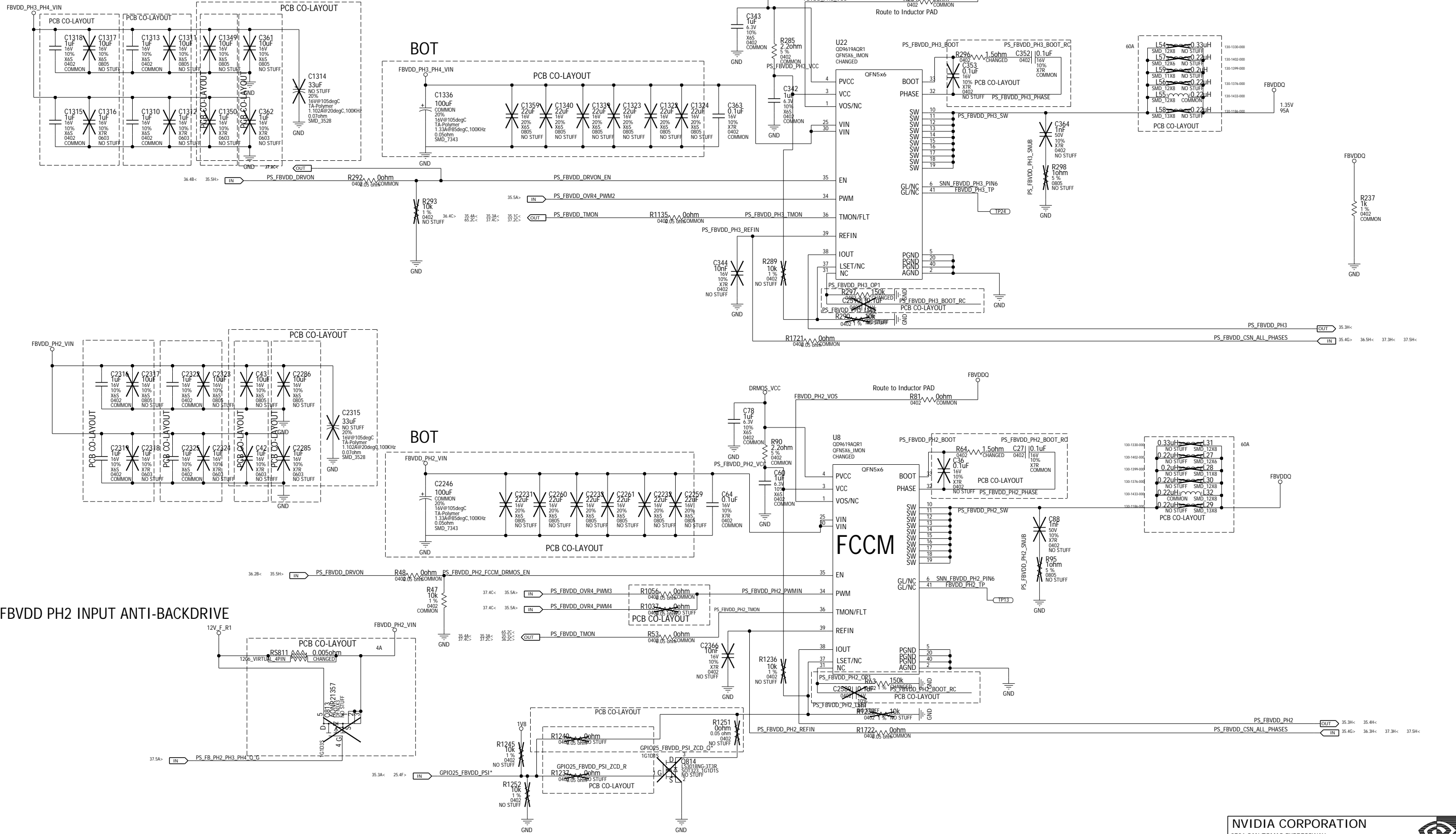
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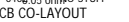
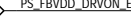
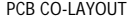
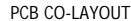
600-1G133-0030-900

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12V_EXT8_F1_R2_RTD3



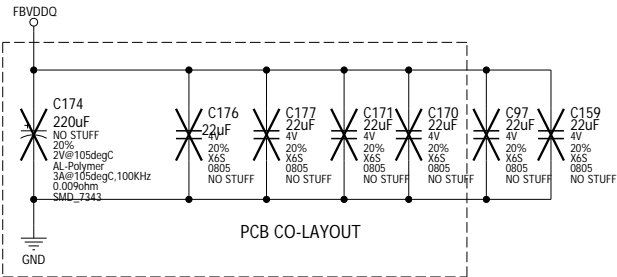
36.5A< OUT IN

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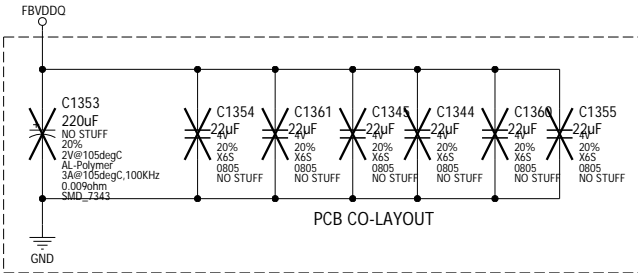
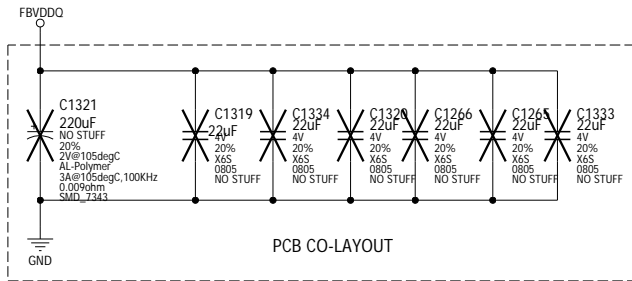
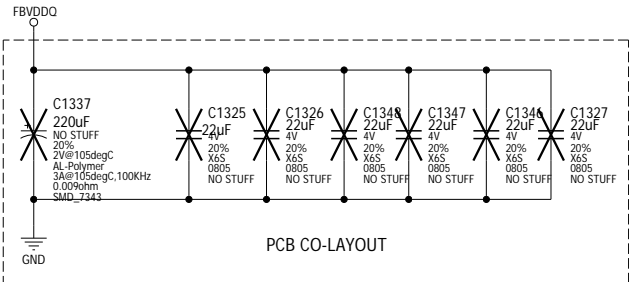
ASSEMBLY	SKU30
PAGE DETAIL	PS: FBVDD PH1 (PWM1) and PH4 (PWM3/4

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PN		600-1G133-0030-900		
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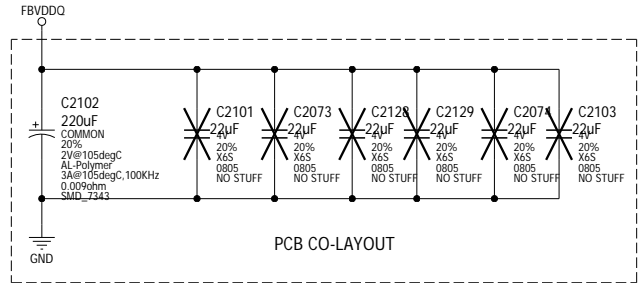
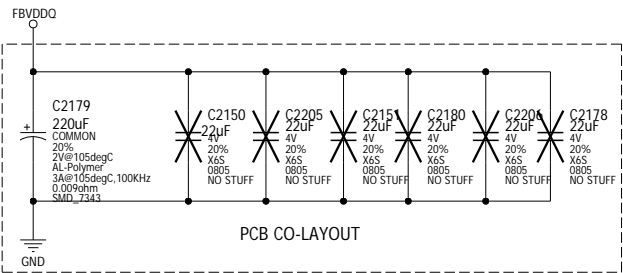
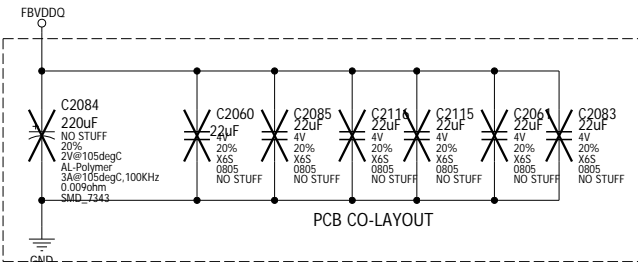
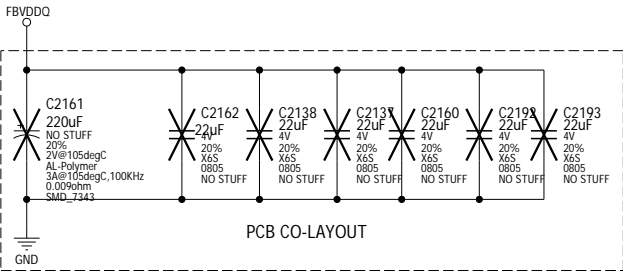
PLACE NEAR POWER SUPPLY
8x SMD7343 330uF CO-LAYOUT WITH 48x 0805 22uF



TOP WEST OF PCB

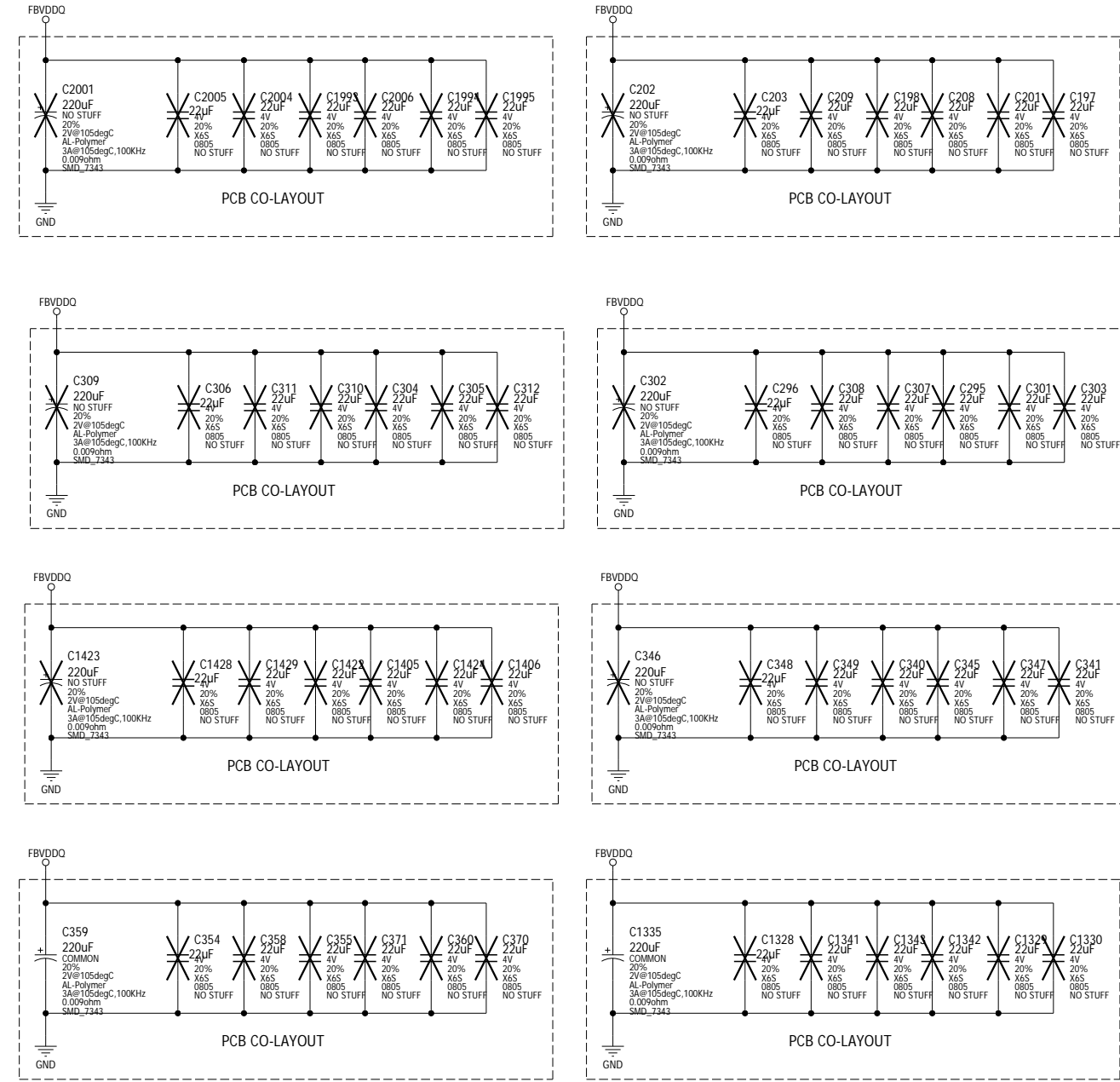


BACK WEST OF PCB



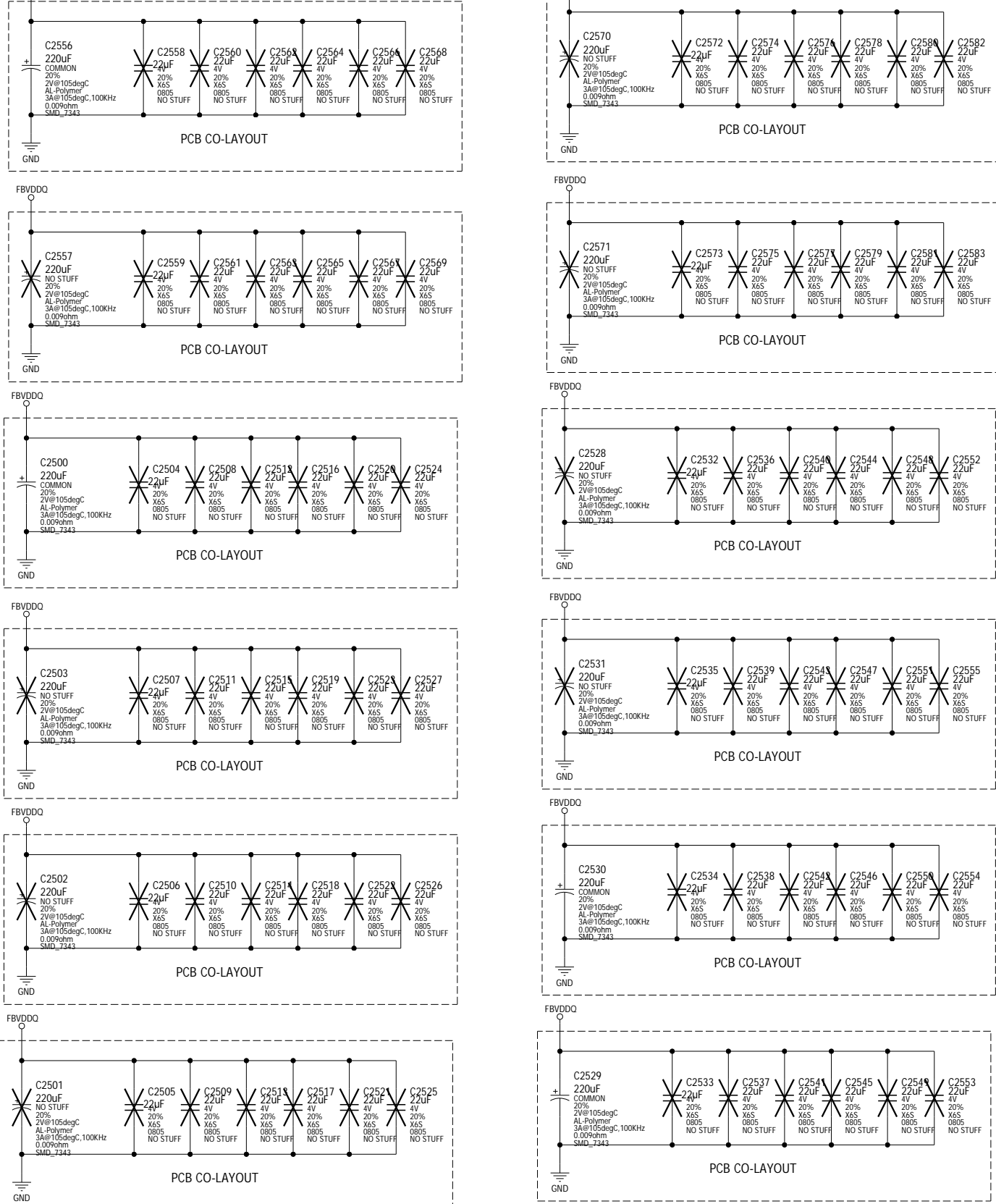
BACK EAST OF PCB

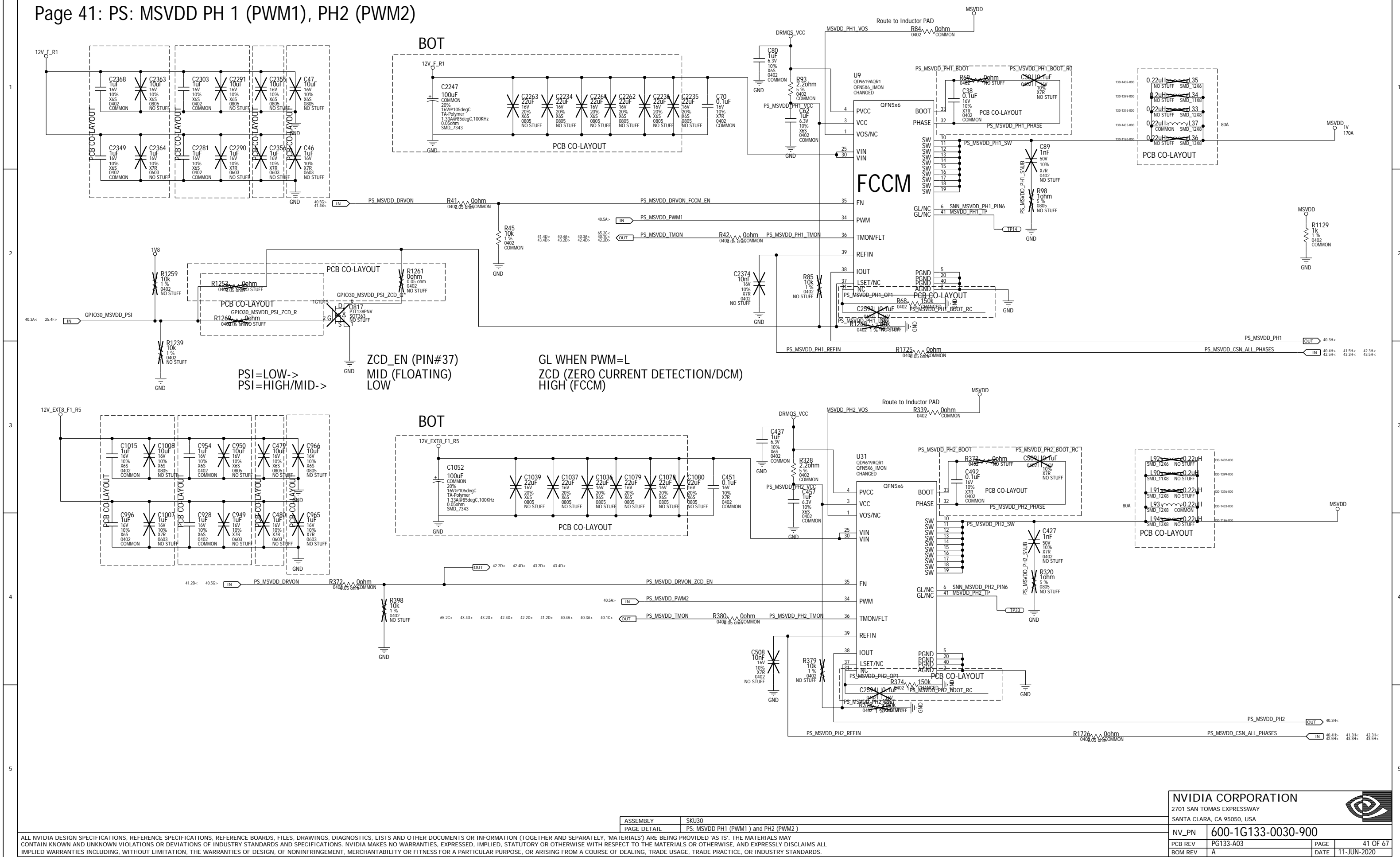
PLACE NEAR MEMORY



Added for A00 x16

ADDED FOR A00 X16 DESIGN: PLACE UNDER MEMORIES



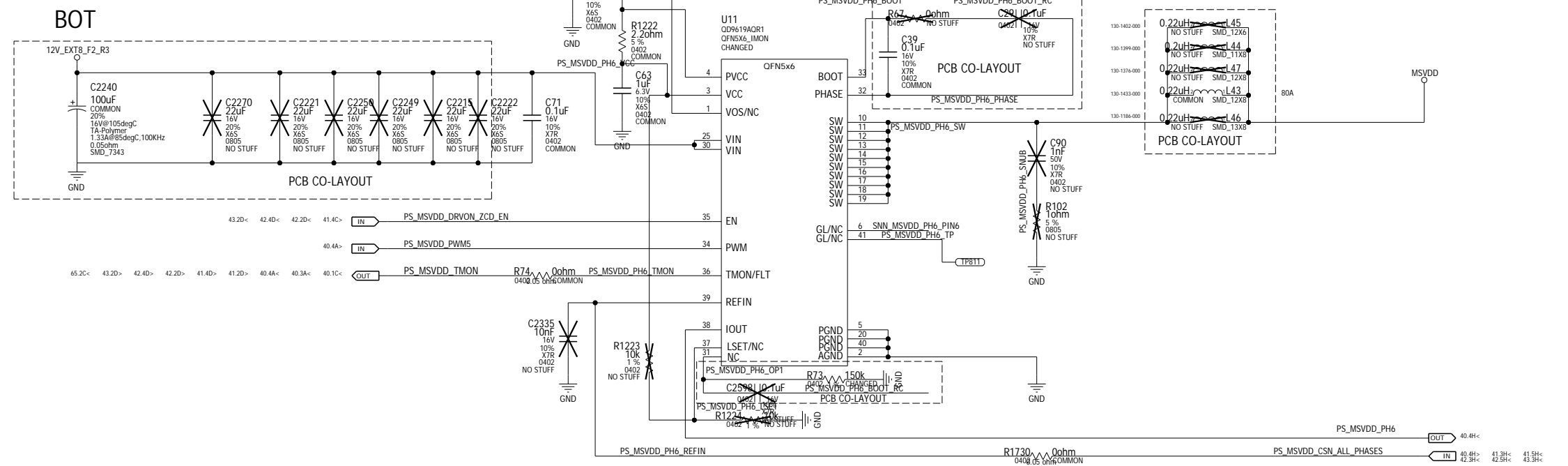
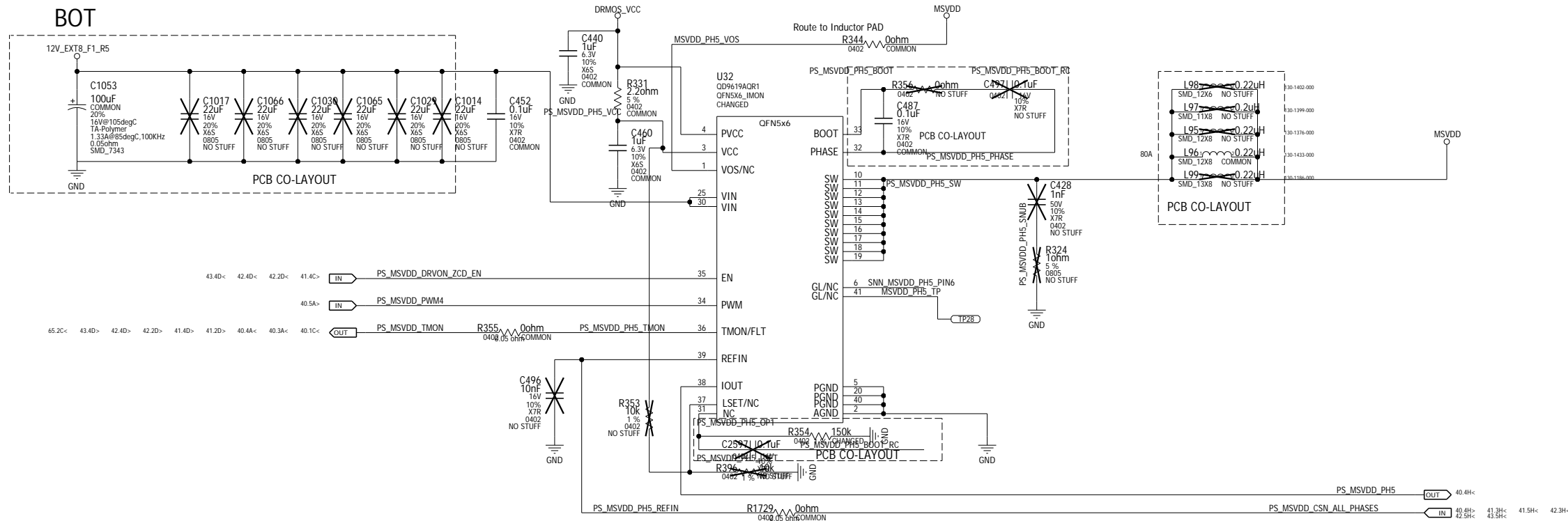
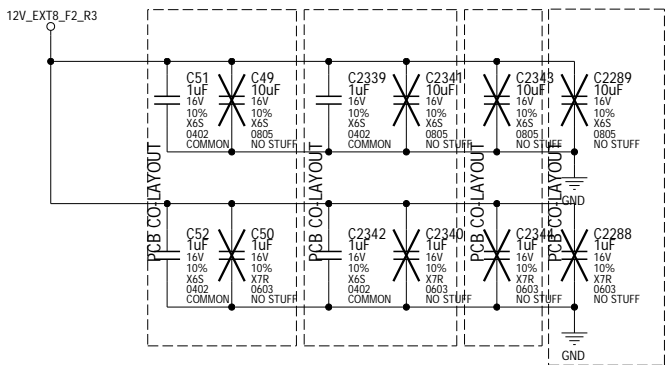
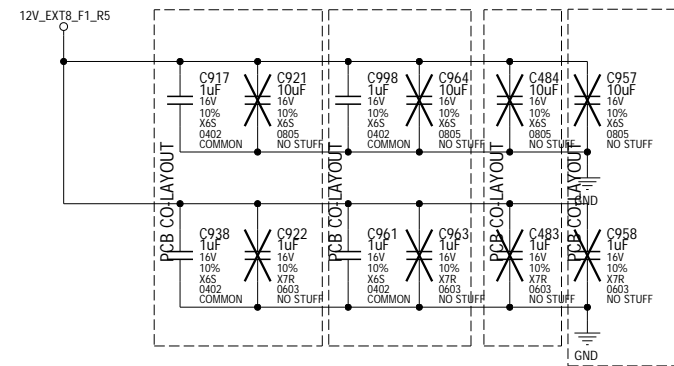




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NV_PN	600-1G133-0030-900		
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Page 43: PS:MSVDD PH 5 (PWM4), PH 6 (PWM5)

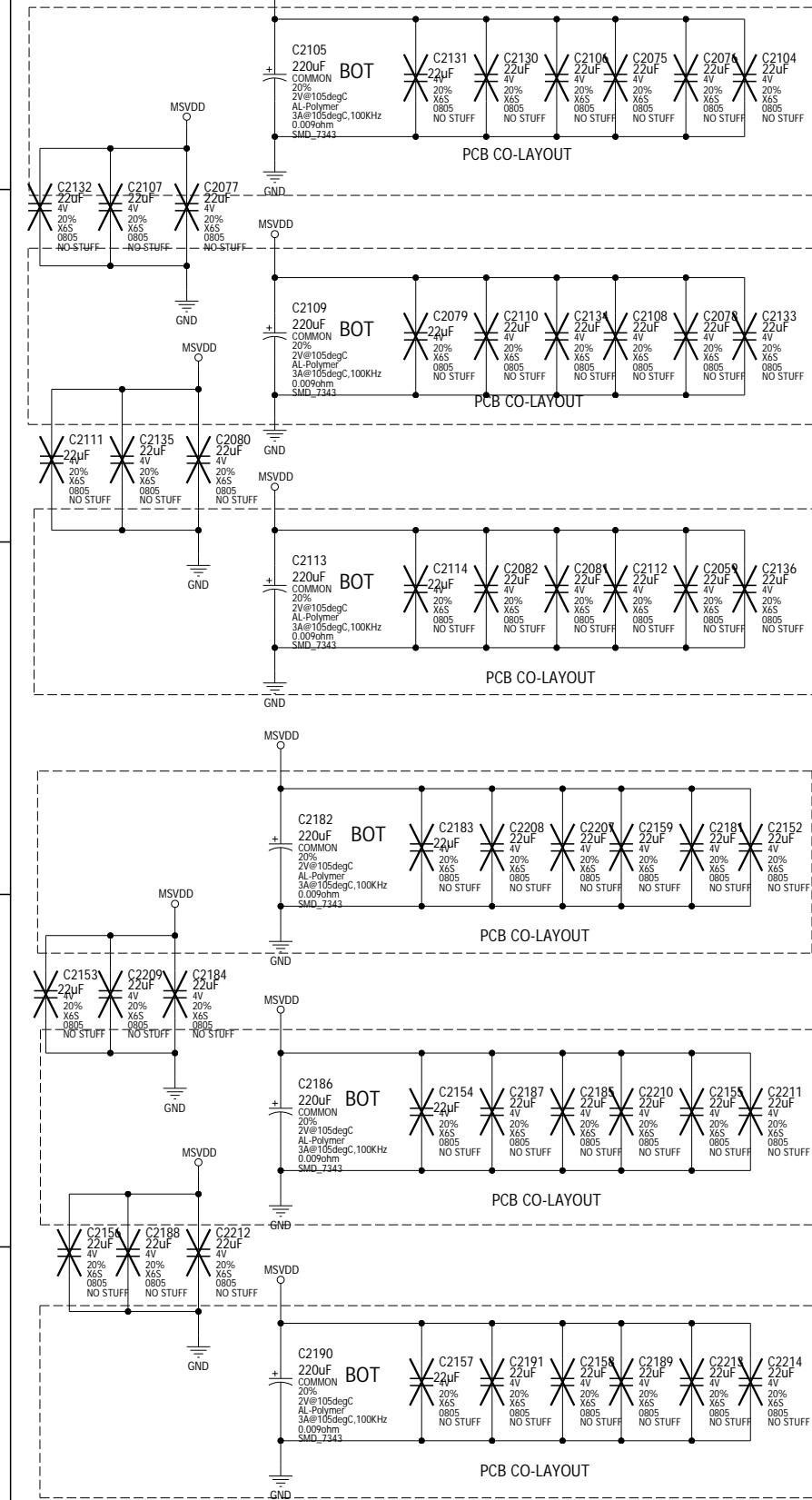


ASSEMBLY	SKU30
PAGE DETAIL	PS: MSVDD PH5 (PWM4) and PH6 (PWM5)

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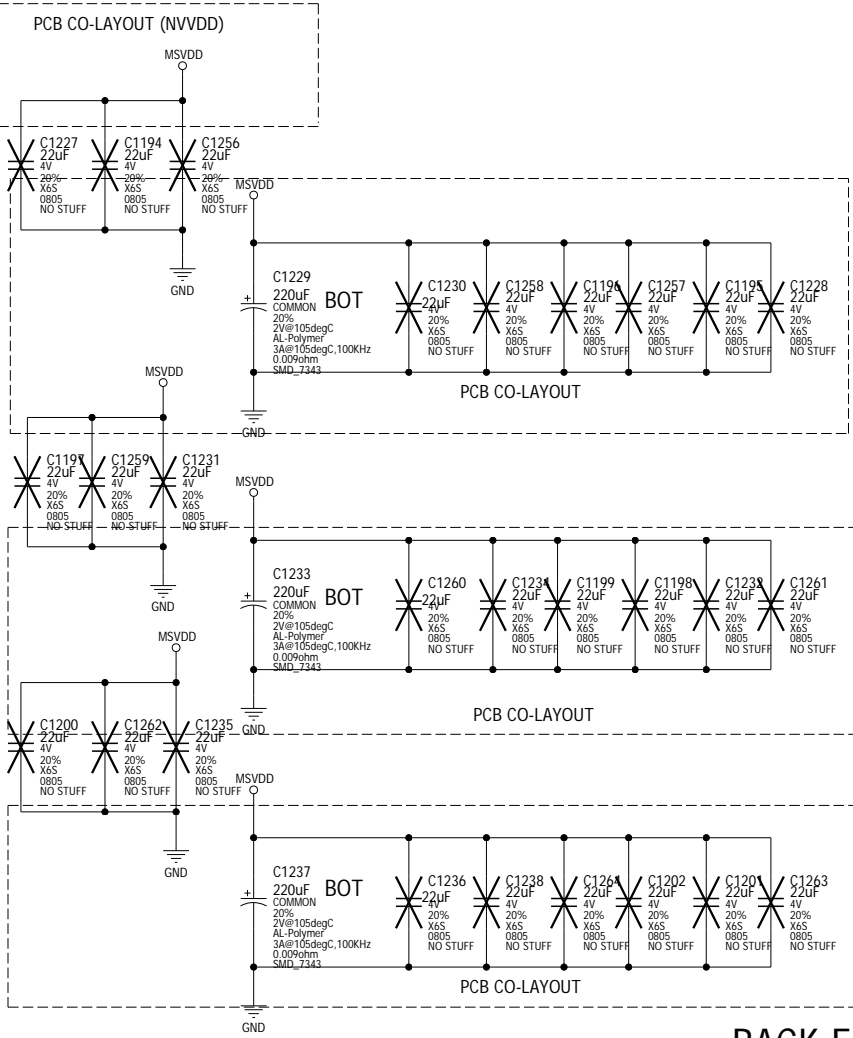
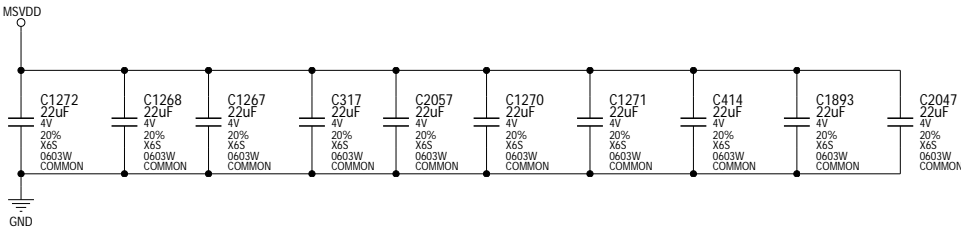
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NV_PN	600-1G133-0030-900			
PCB REV	P133-A03	PAGE	43 OF 67	
BOM REV	A	DATE	11-JUN-2020	

Page 44: PS: MSVDD OUTPUT CAP
12x SMD7343 330uF CO-LAYOUT WITH 72x 0805 22uF

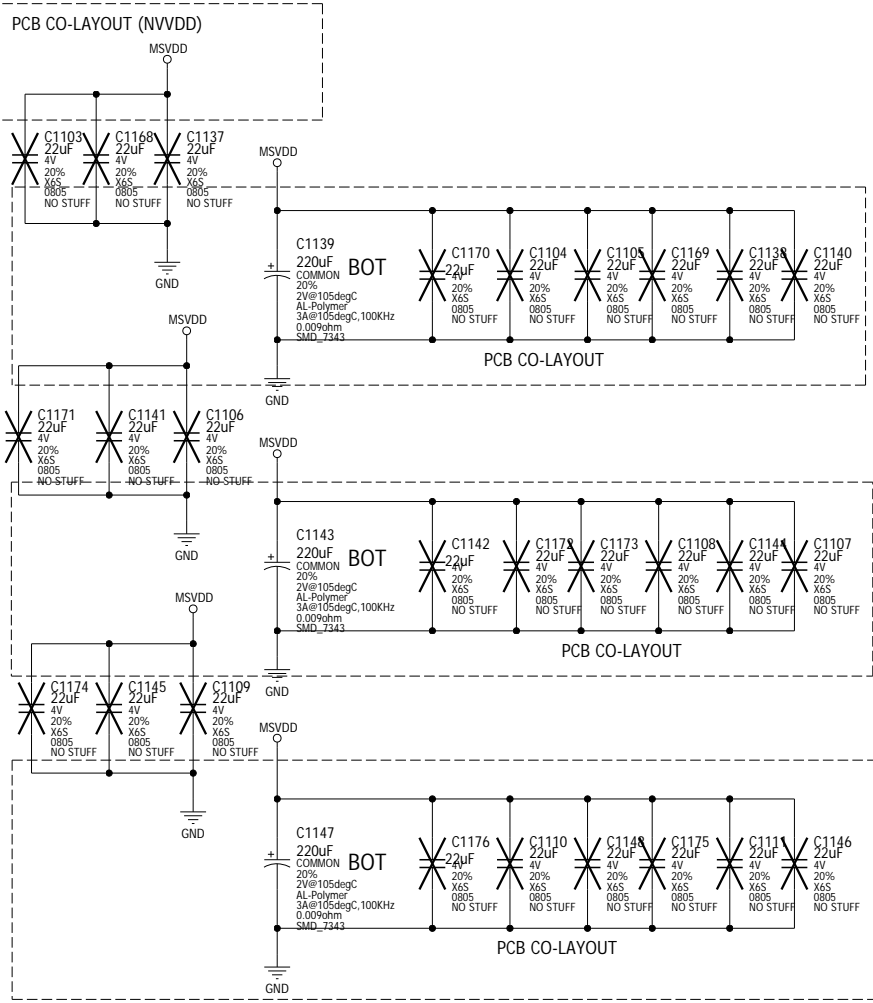
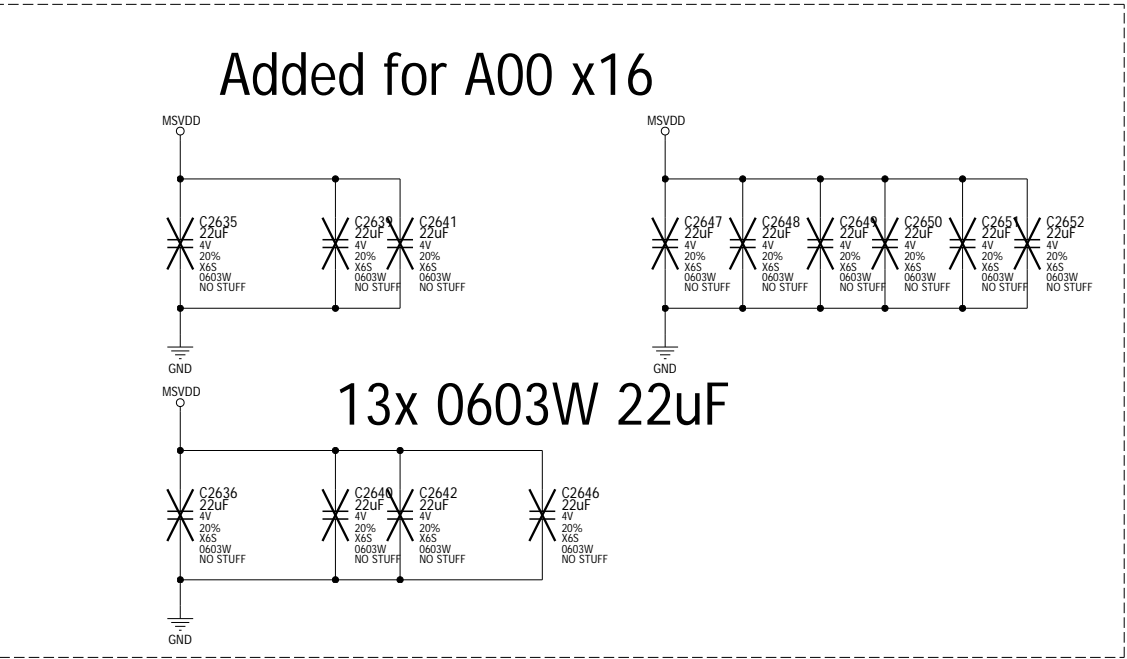


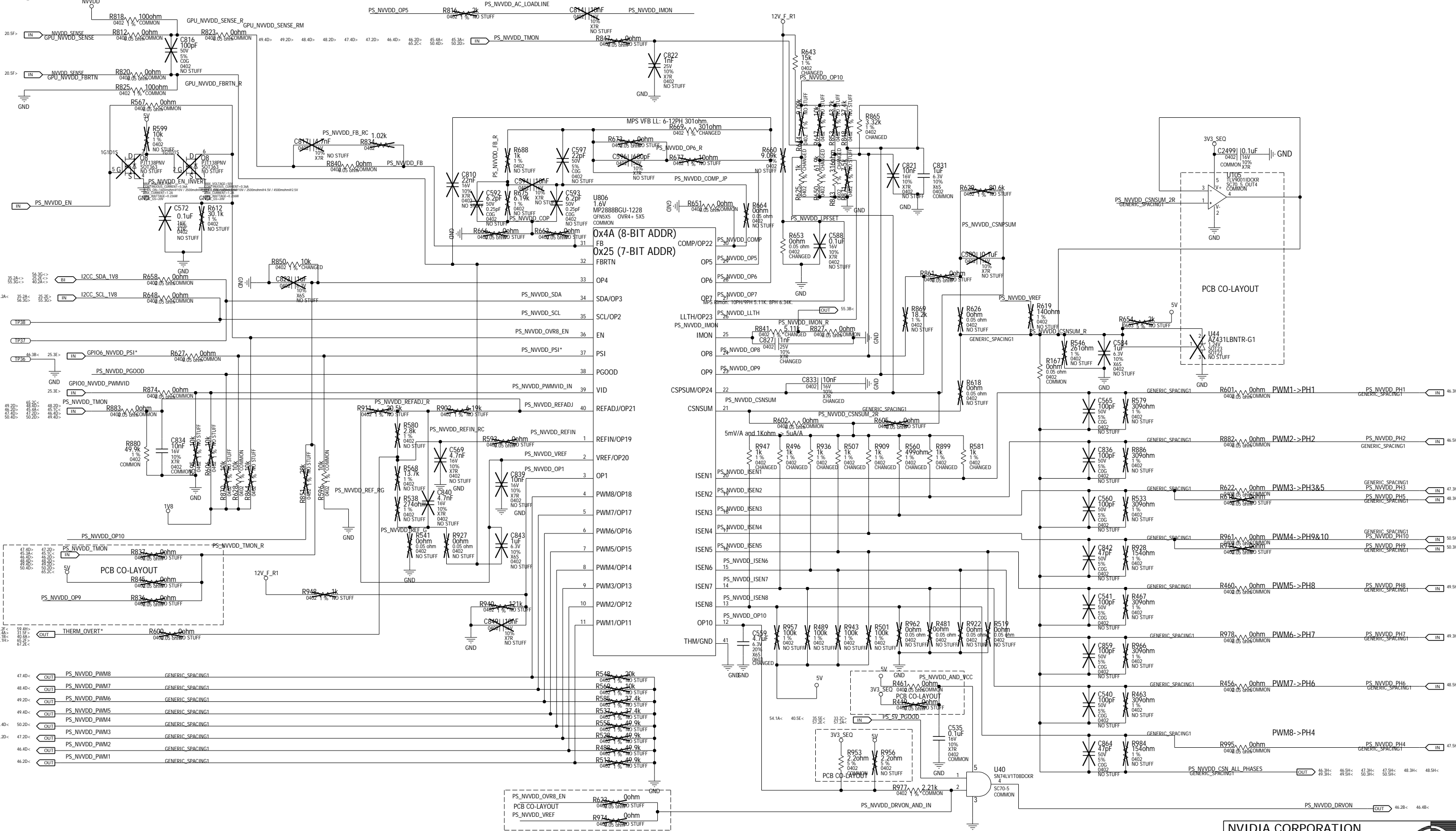
BACK WEST OF PCB

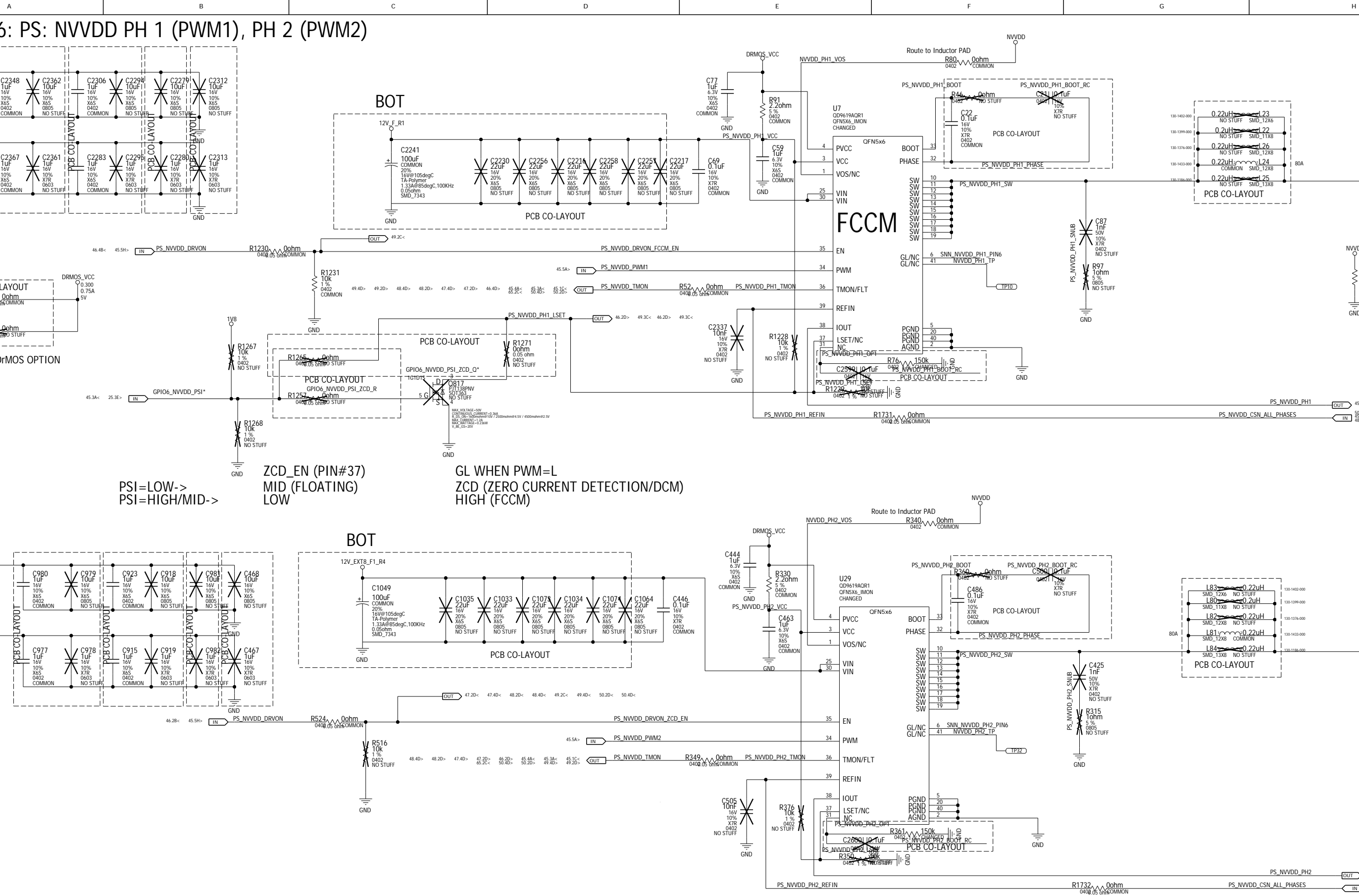
10x 0603W 22uF BETWEEN GPU AND VRM



BACK EAST OF PCB

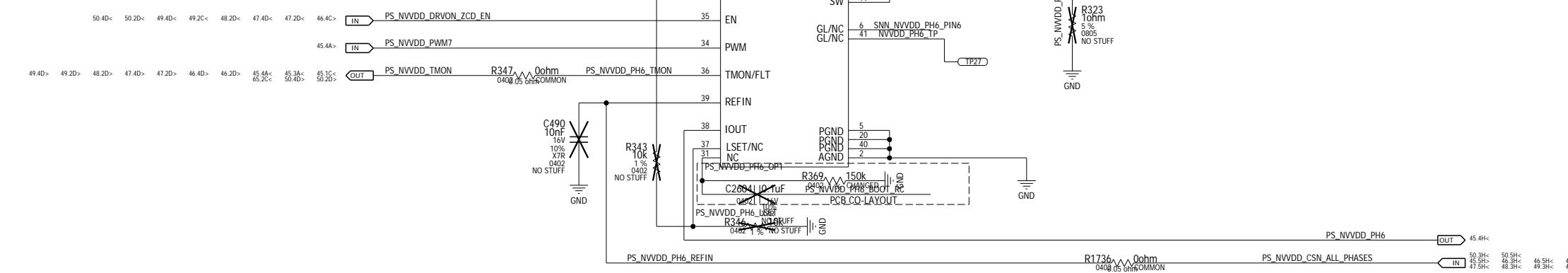
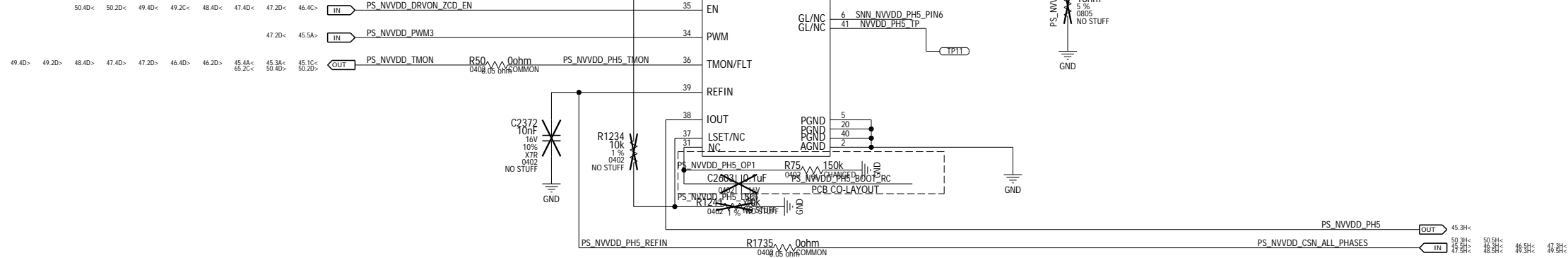
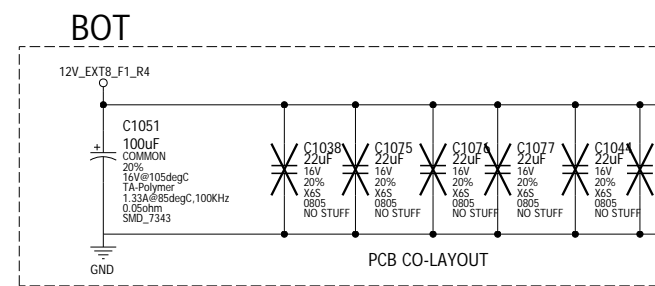
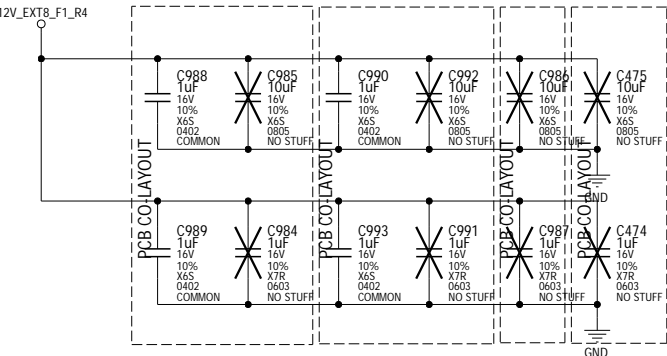
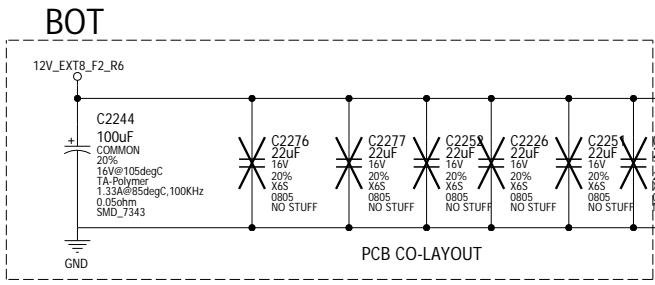
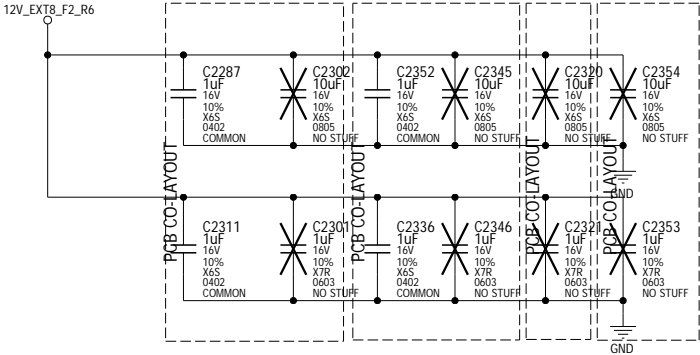




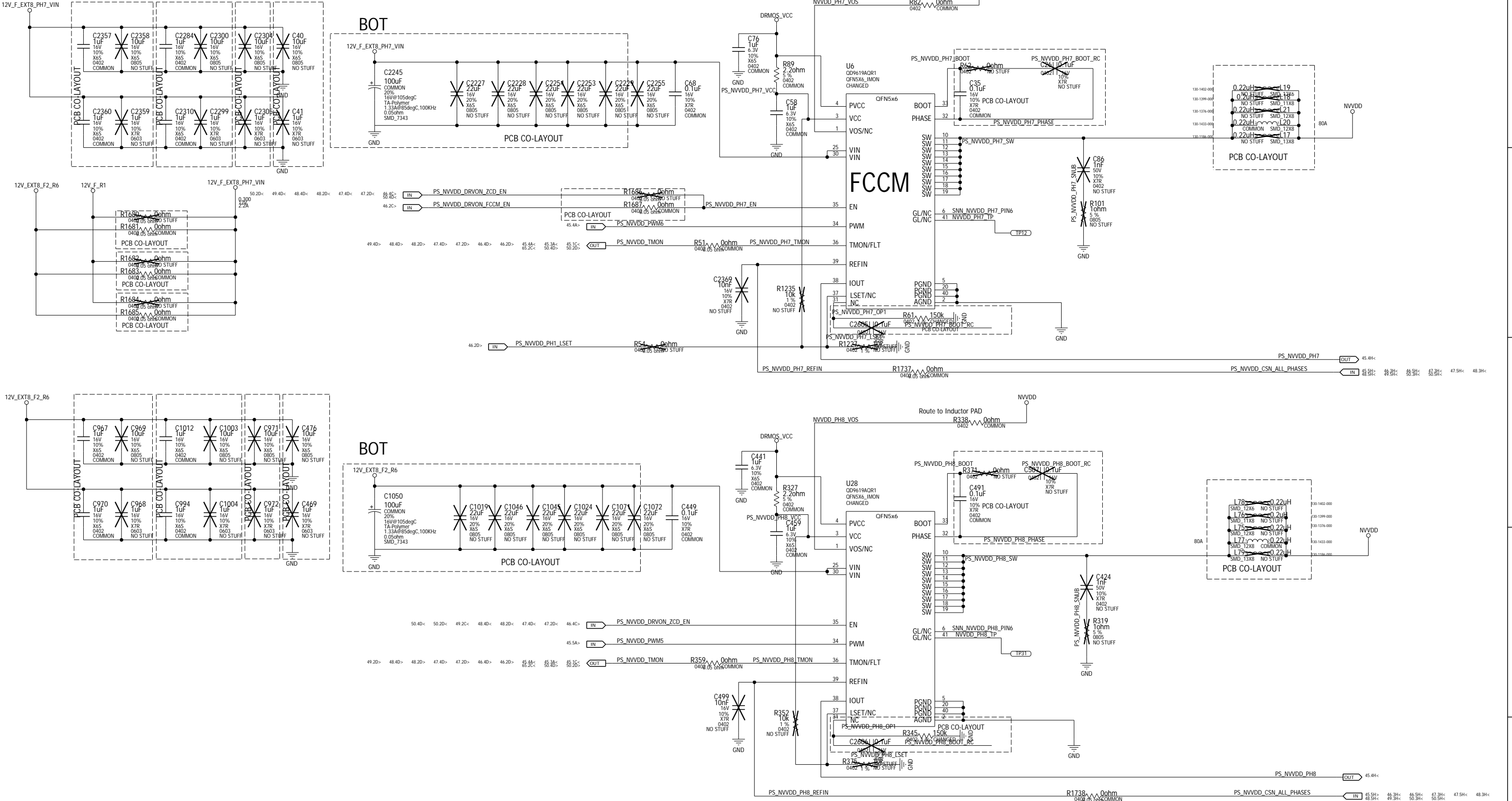


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ASSEMBLY	SKU30	NV_PN	600-1G133-0030-90
PAGE DETAIL	PS: NVVDD PH1 (PWM1) and PH2 (PWM2)	PCB REV	PG133-A03
		BOM REV	A

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PCB REV	PG133-A03				
BOM REV	A				



Page 49: PS: NVVDD PH 7 (PWM6), PH8 (PWM5)



ASSEMBLY	SKU30
PAGE DETAIL	PS: NVVDD PH7 (PWM6) and PH8 (PWM5)

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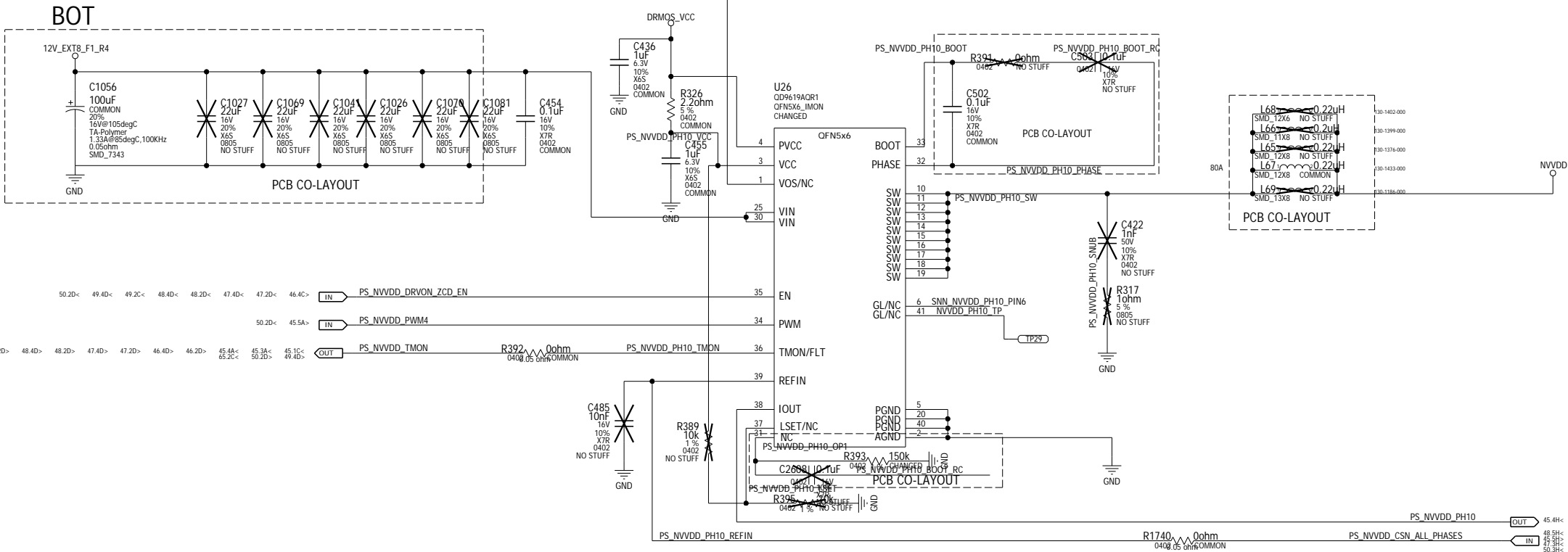
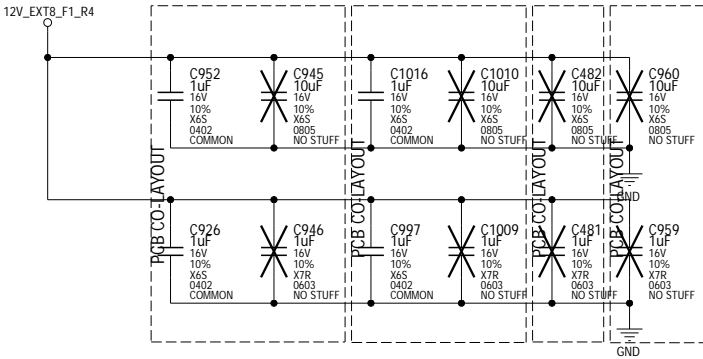
2701 SAN TOMAS EXPRESSWAY

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NV_PN	600-1G133-0030-900
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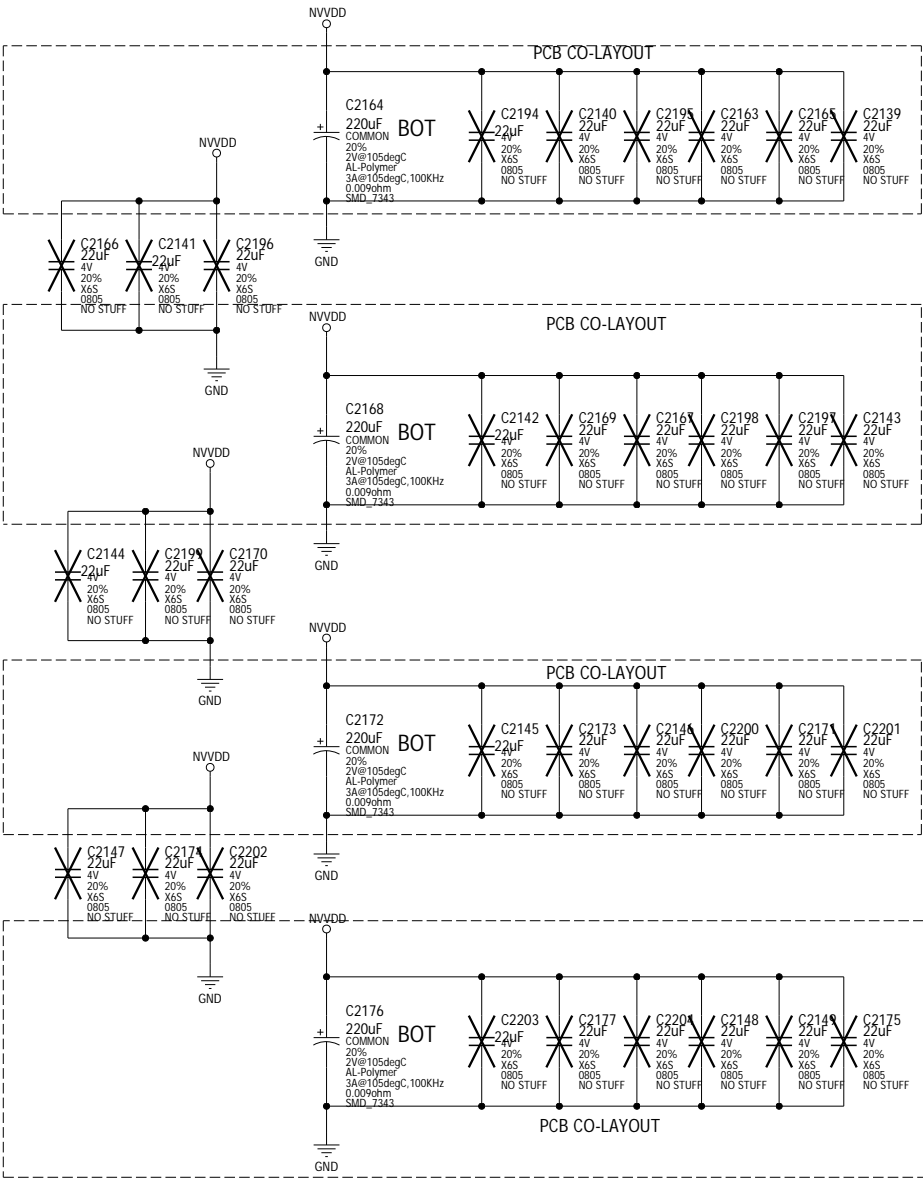
PCB REV	PG133-A03	PAGE	49 OF 67
BOM REV	A	DATE	11-JUN-2020



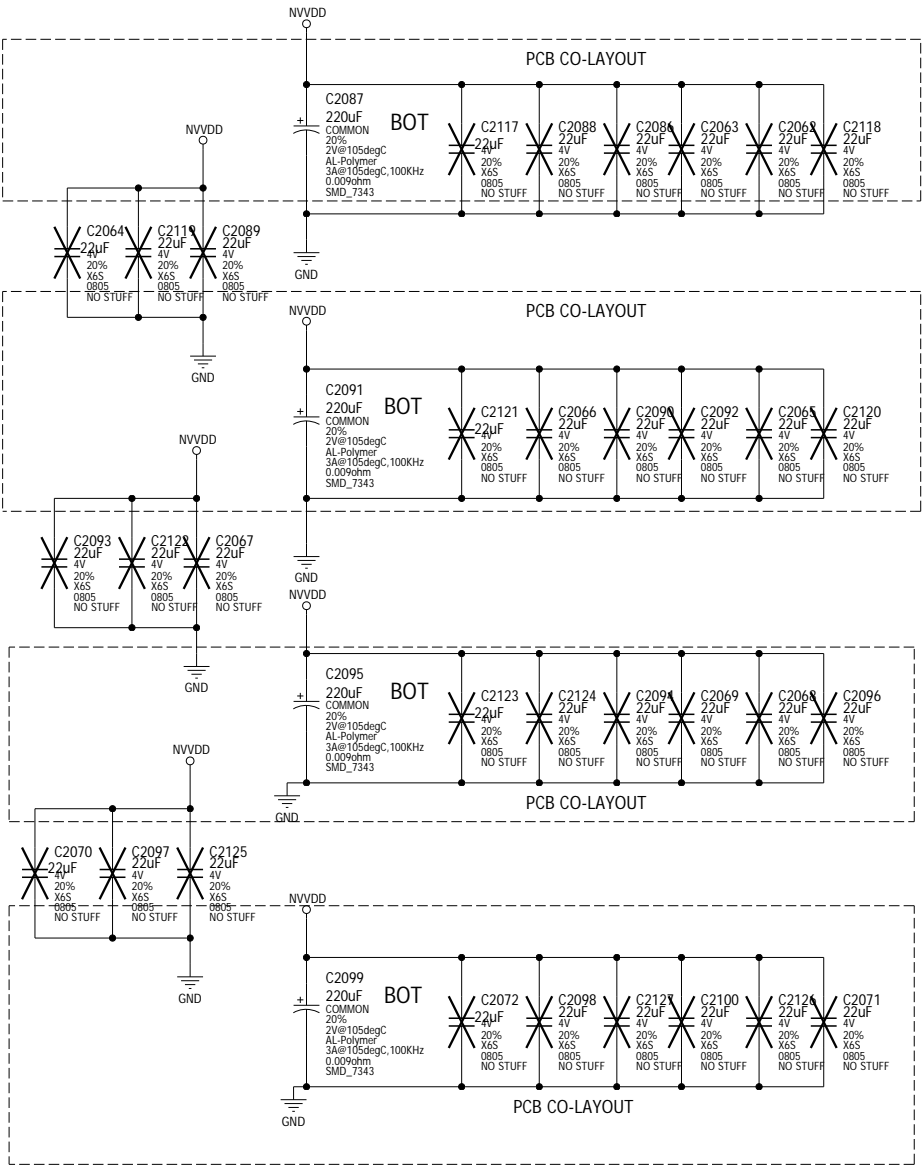
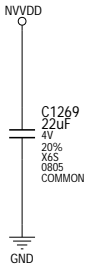
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
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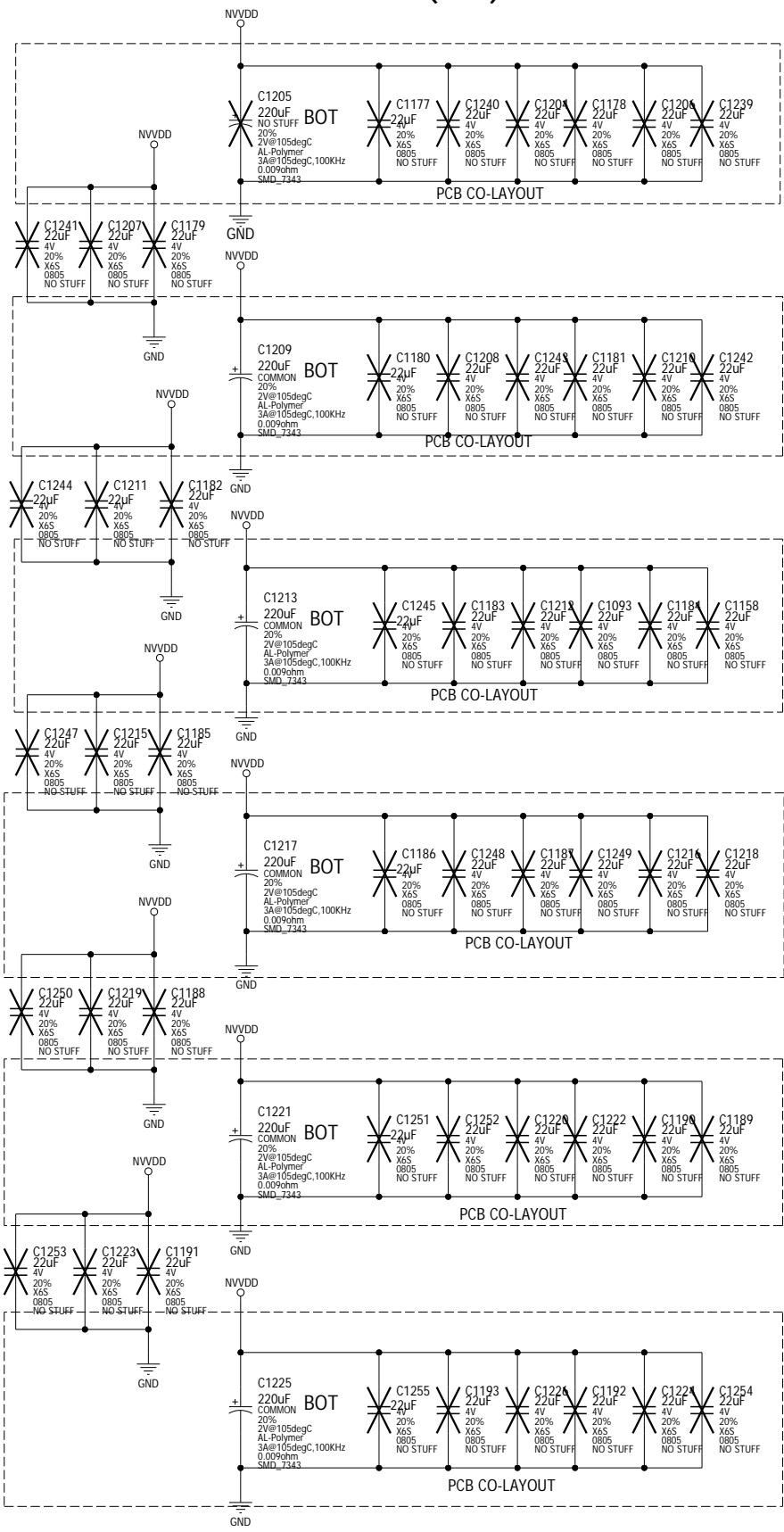
20x SMD7343 220uF CO-LAYOUT WITH 120x 0805 22uF



BACK WEST OF PCB

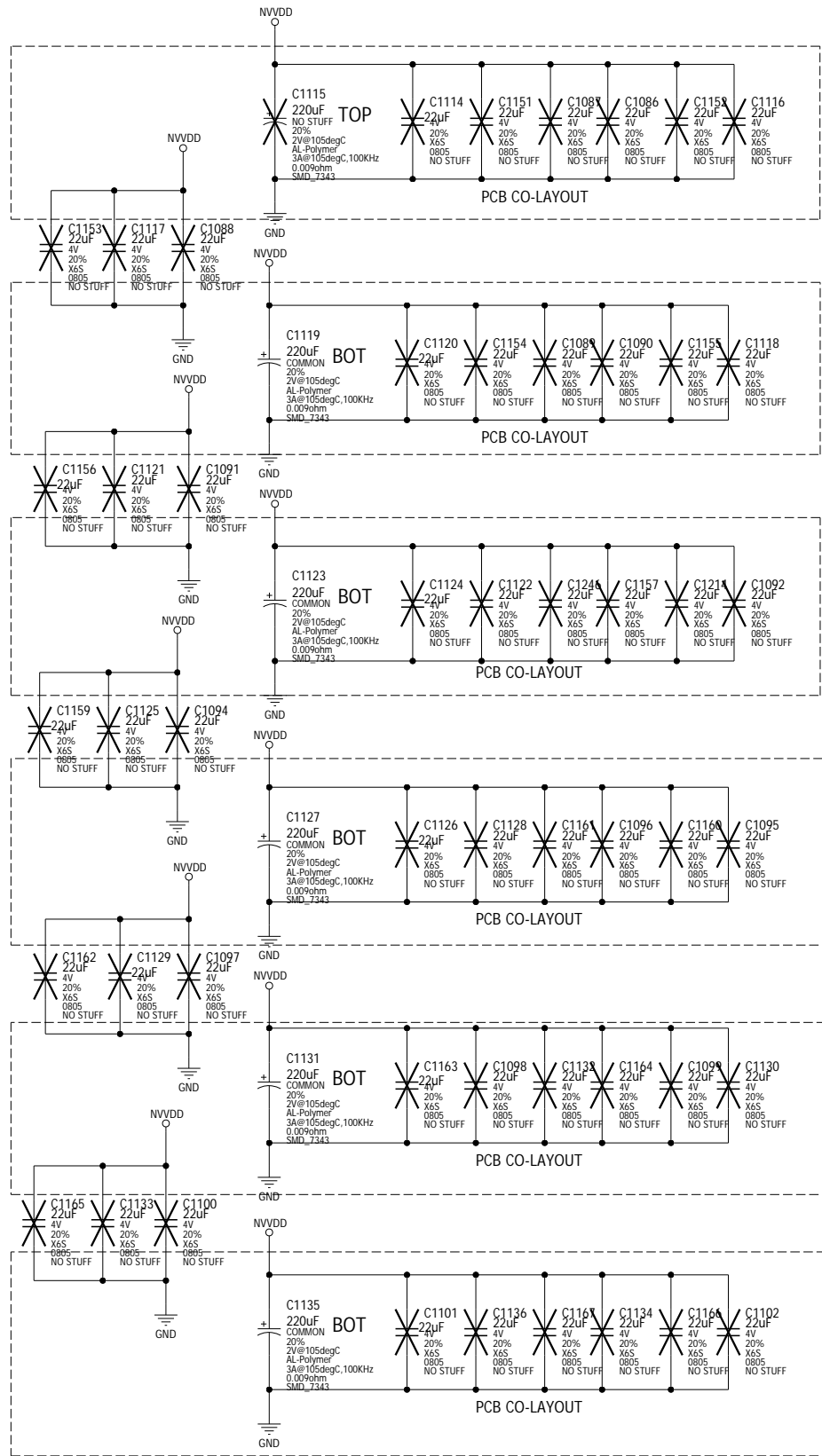
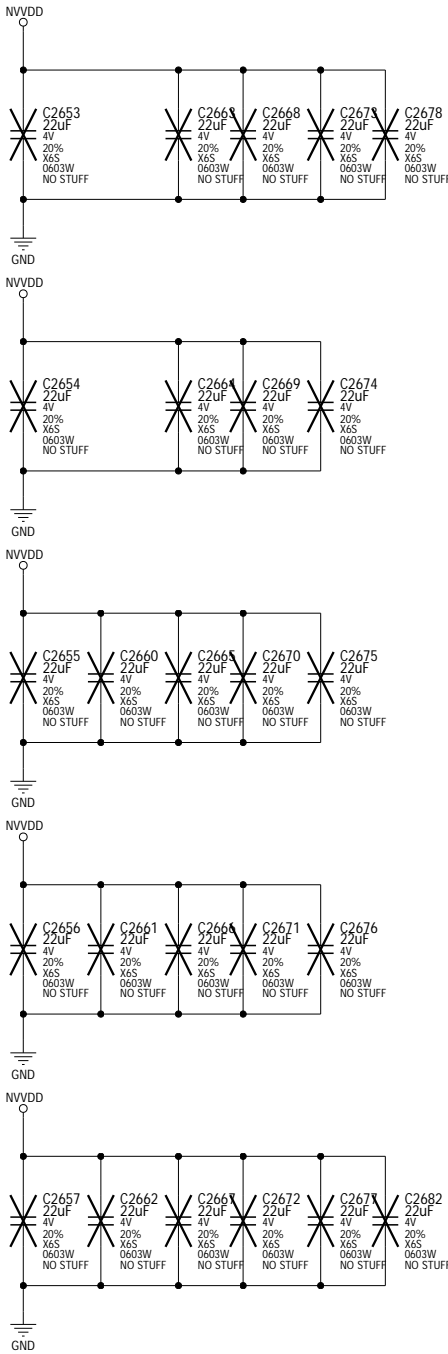


BACK WEST OF PCB



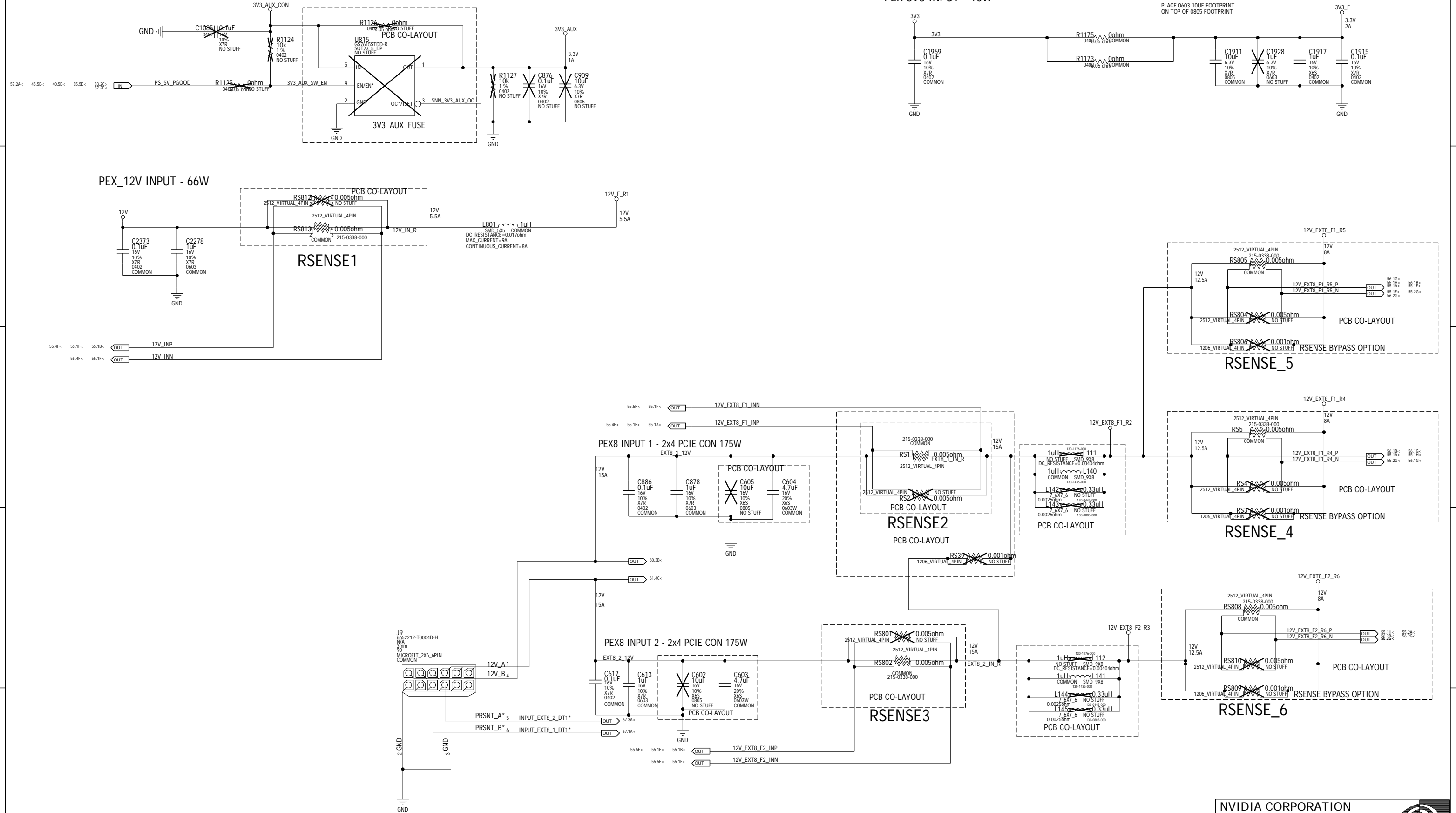
BACK EAST OF PCB

Added for A00 x16
25x 0603W 22uF

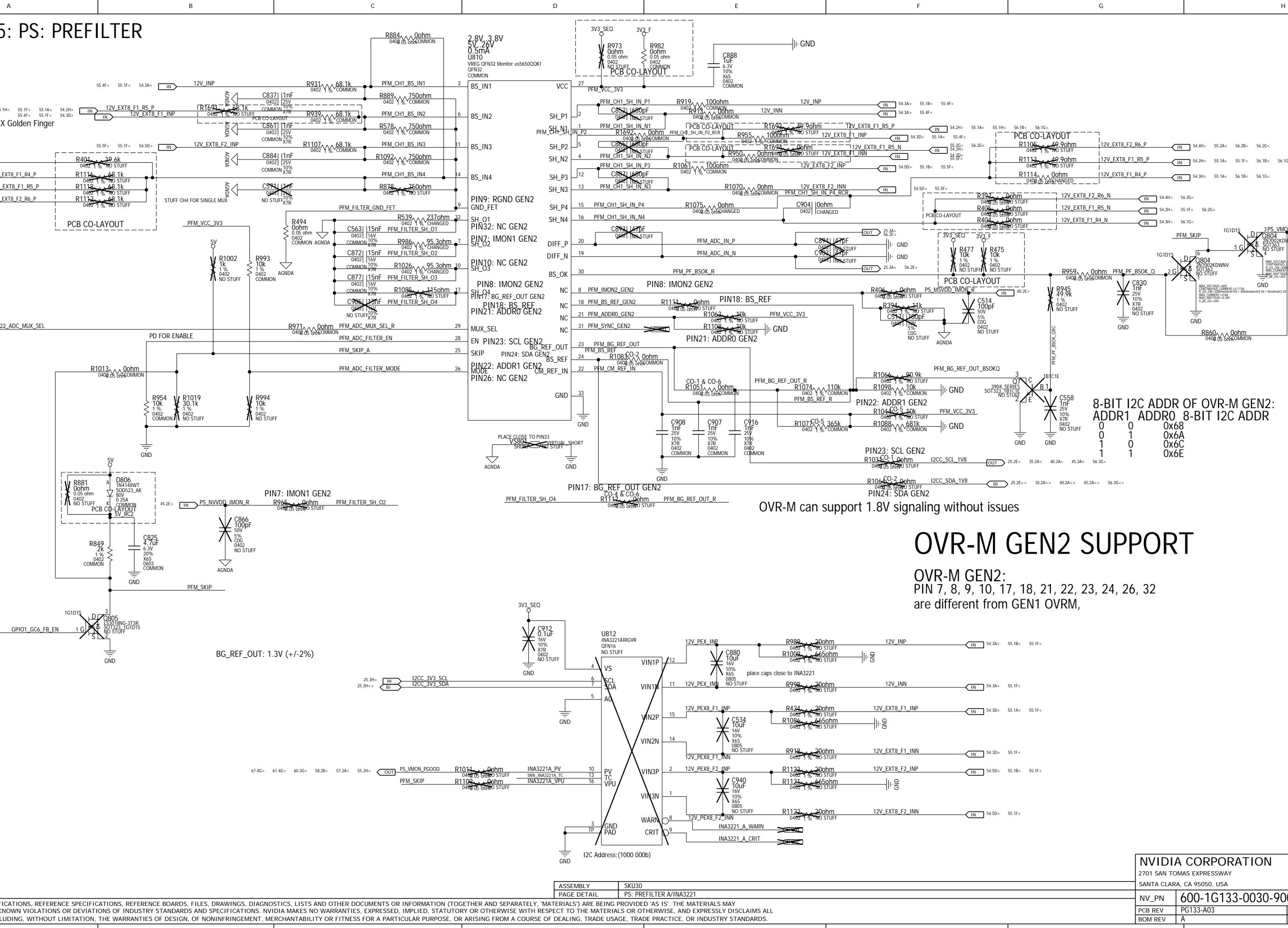


BACK EAST OF PCB

Page 54: PS: INPUTS, FILTERING, MONITORING



A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---



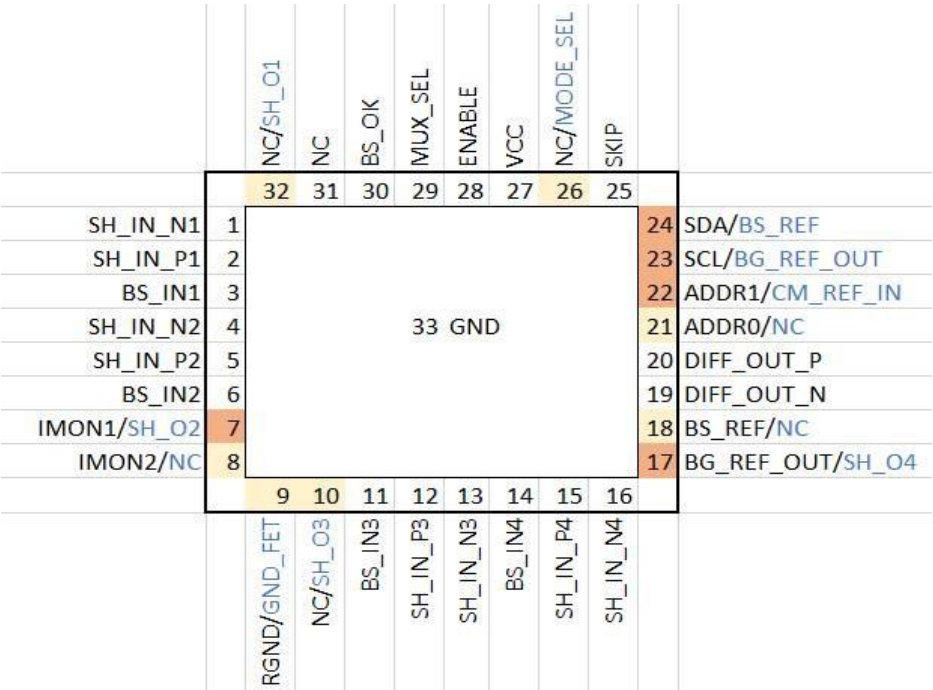
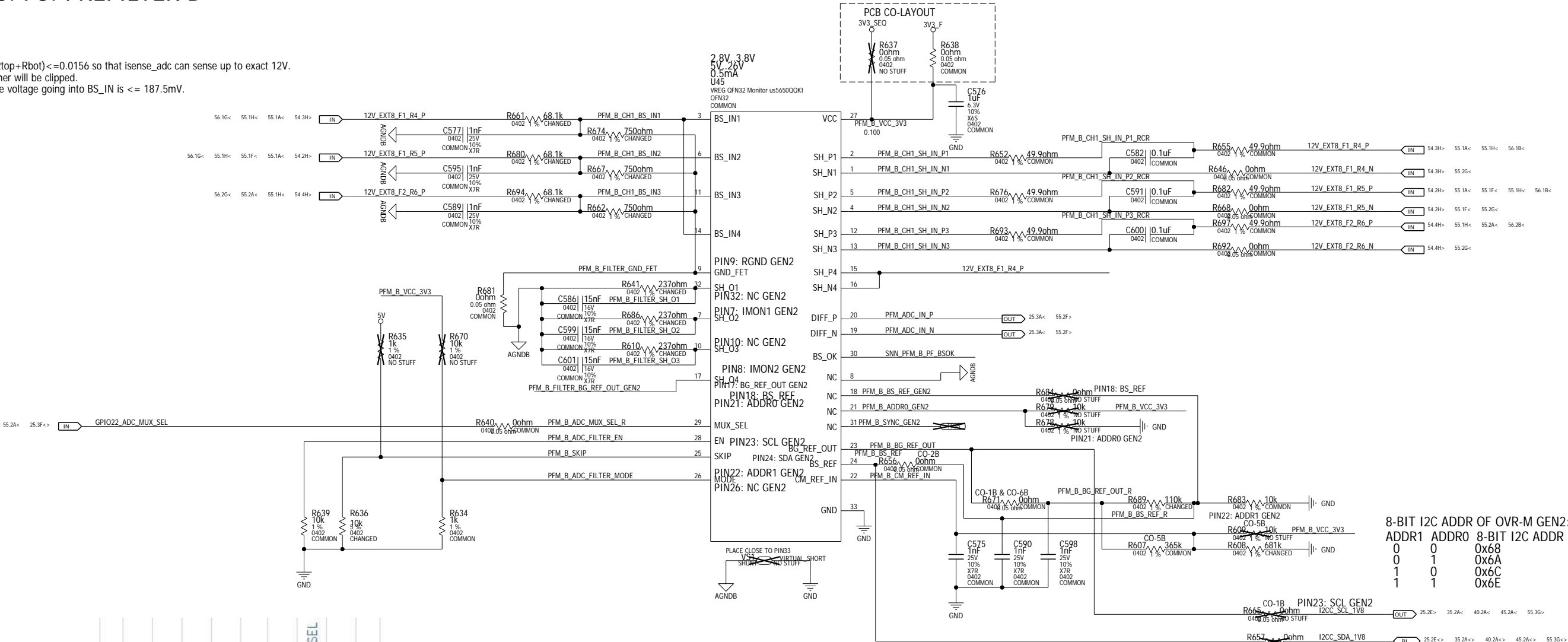
A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---

A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---

A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---

A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---

BUS: $R_{bot}/(R_{top}+R_{bot}) \leq 0.0156$ so that `isense_adc` can sense up to exact 12V.
Anything higher will be clipped.
Make sure the voltage going into `BS_IN` is $\leq 187.5mV$.

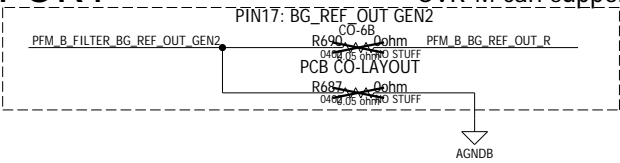


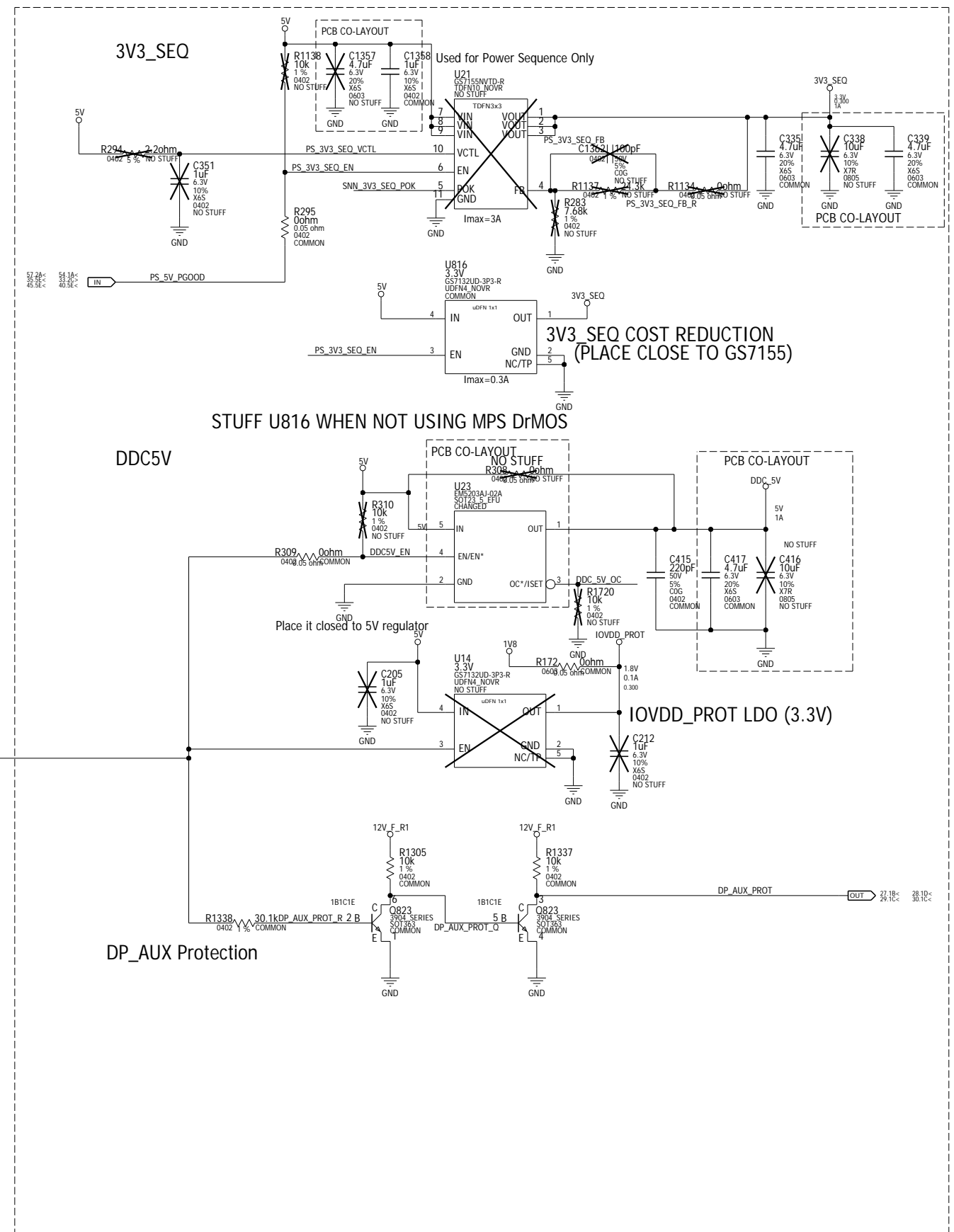
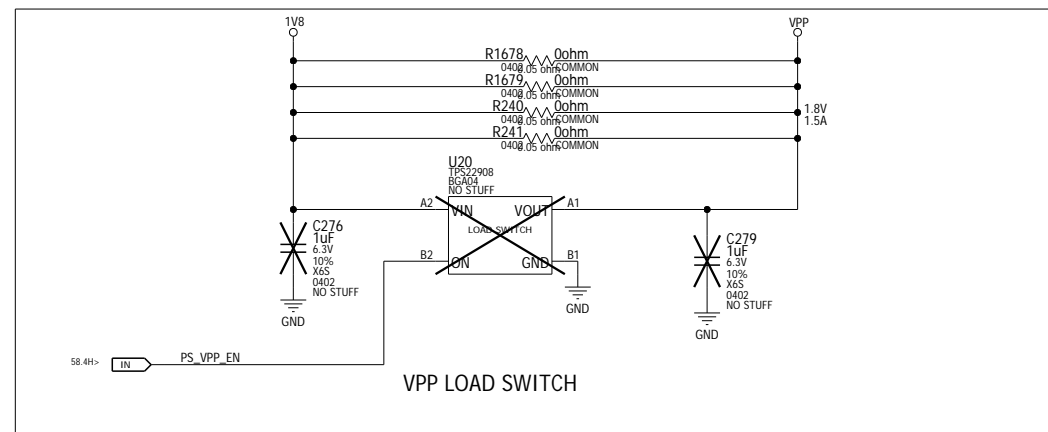
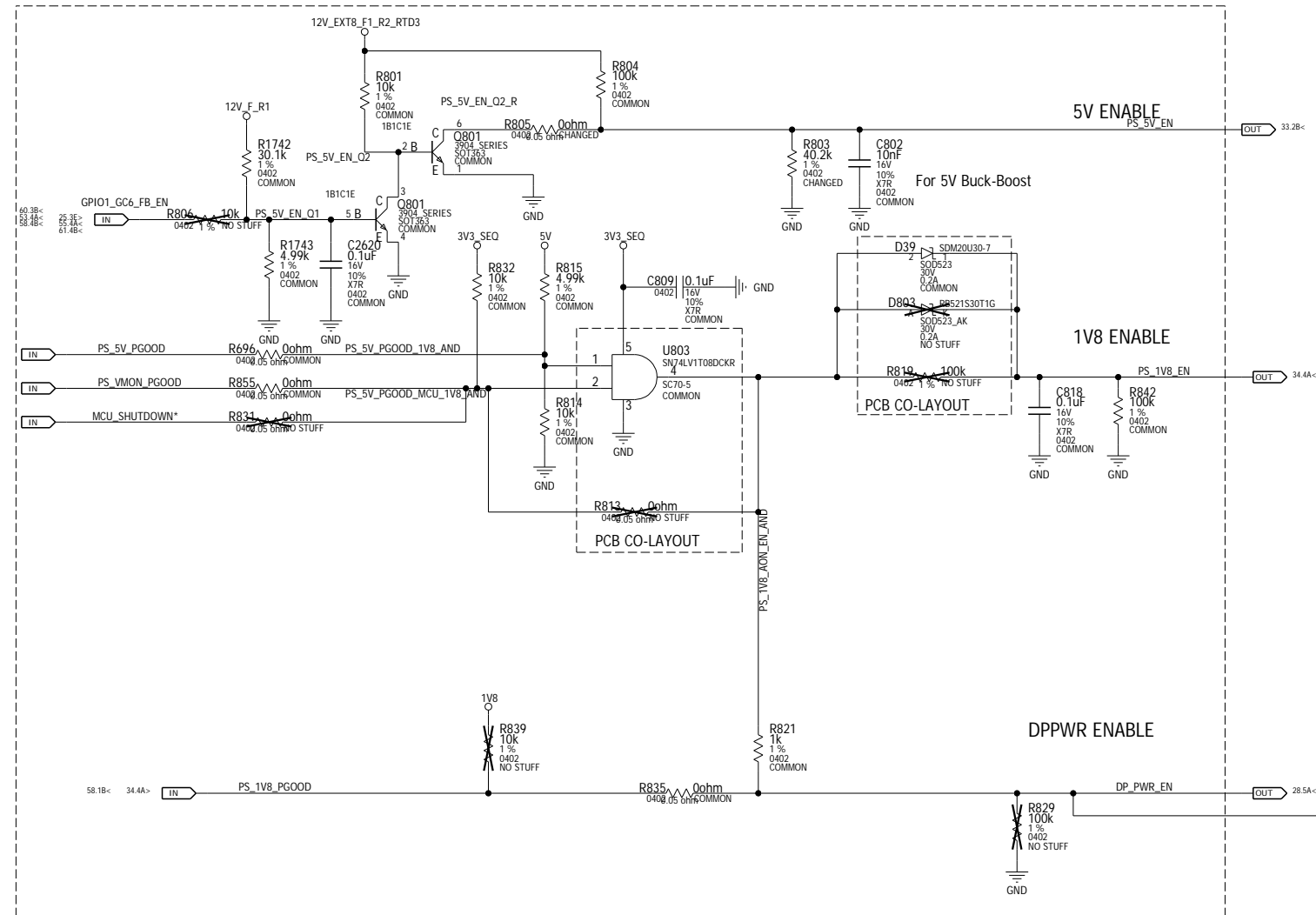
OVR-M GEN2 SUPPORT

OVR-M GEN2:

PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32
are different from GEN1 OVRM,

OVR-M can support 1.8V signaling without issues





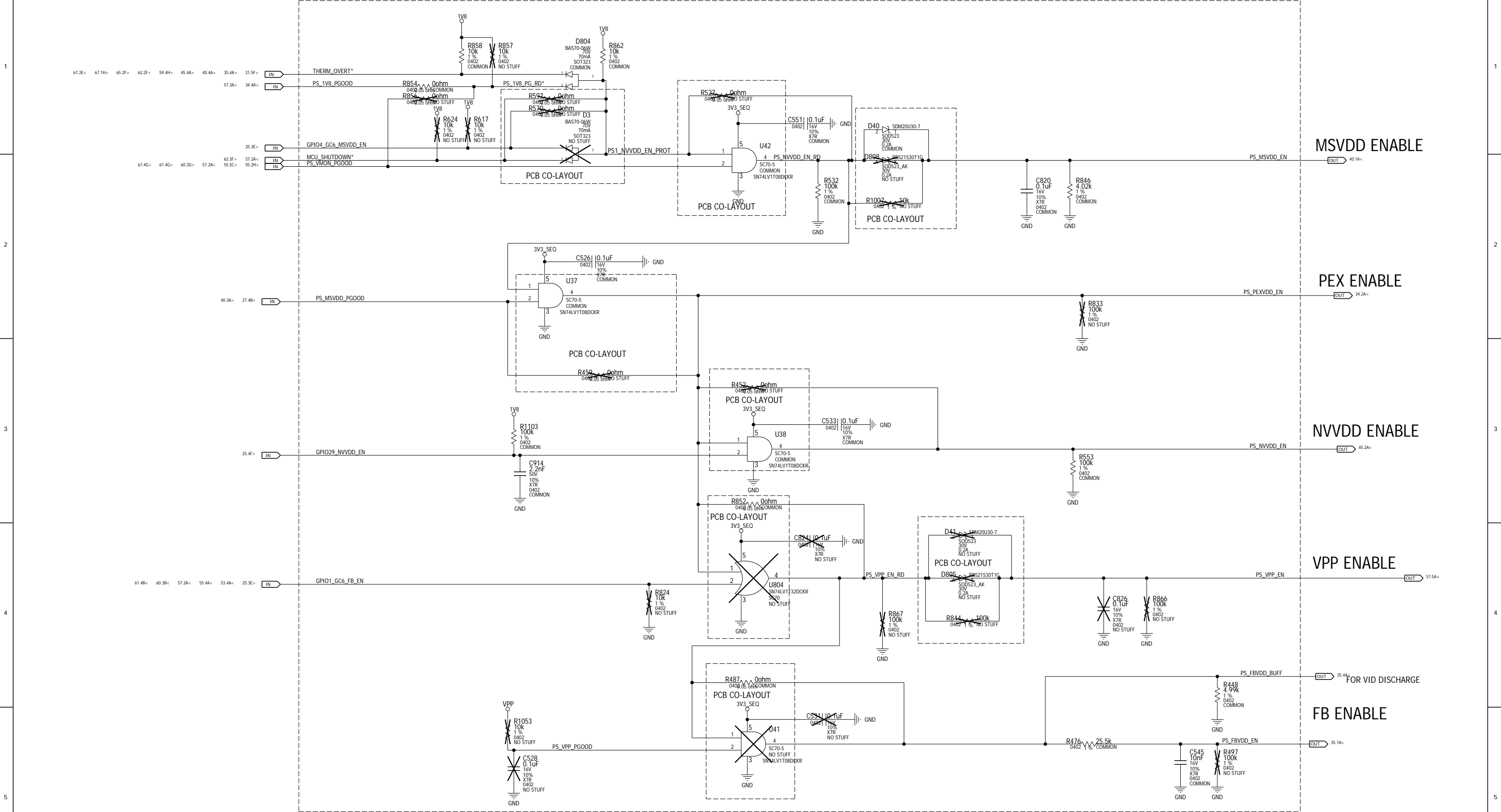
ASSEMBLY	SKU30
PAGE DETAIL	SEQ: 5V/1V8 EN & VPP LOAD SW

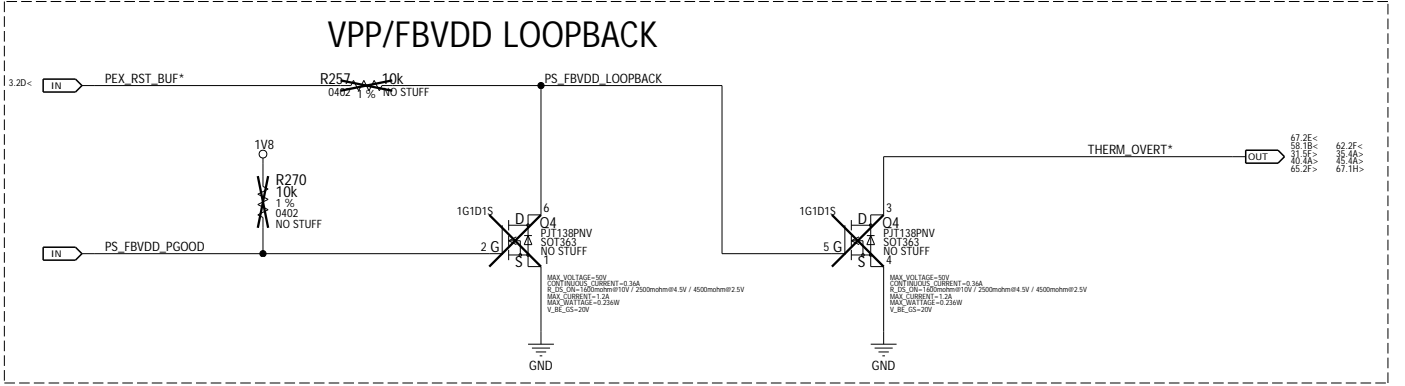
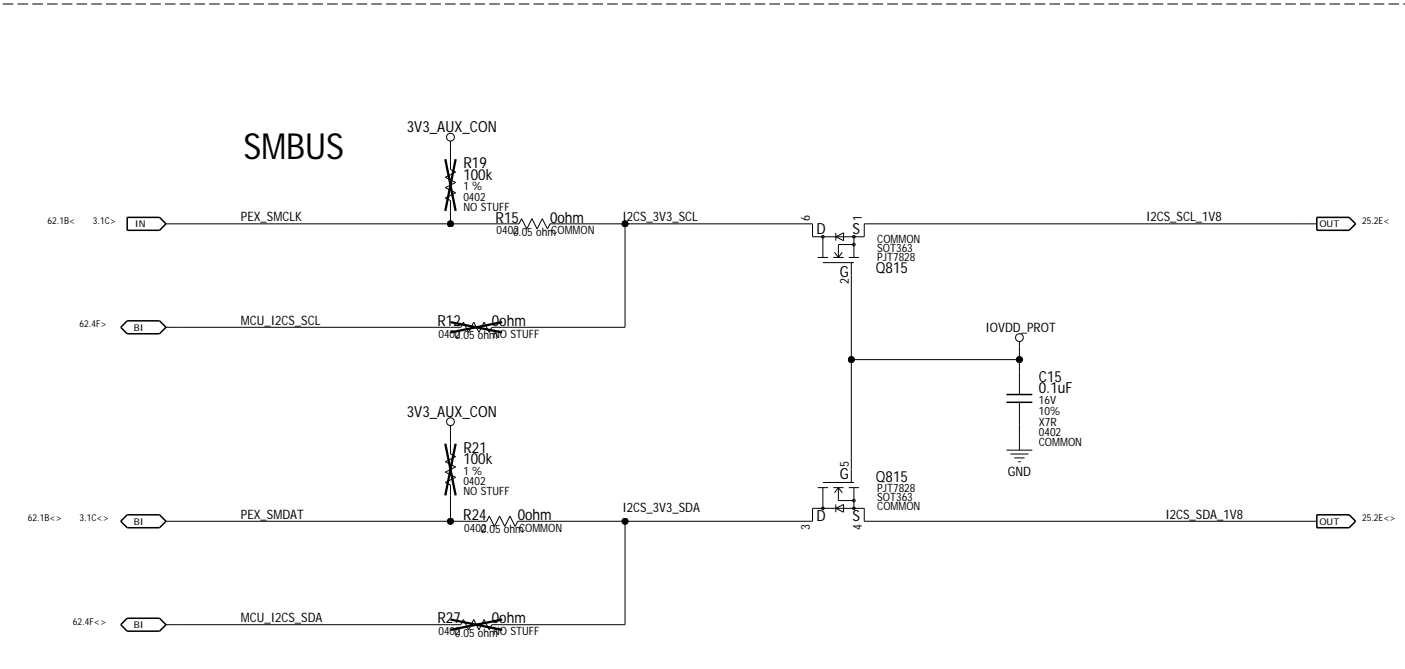
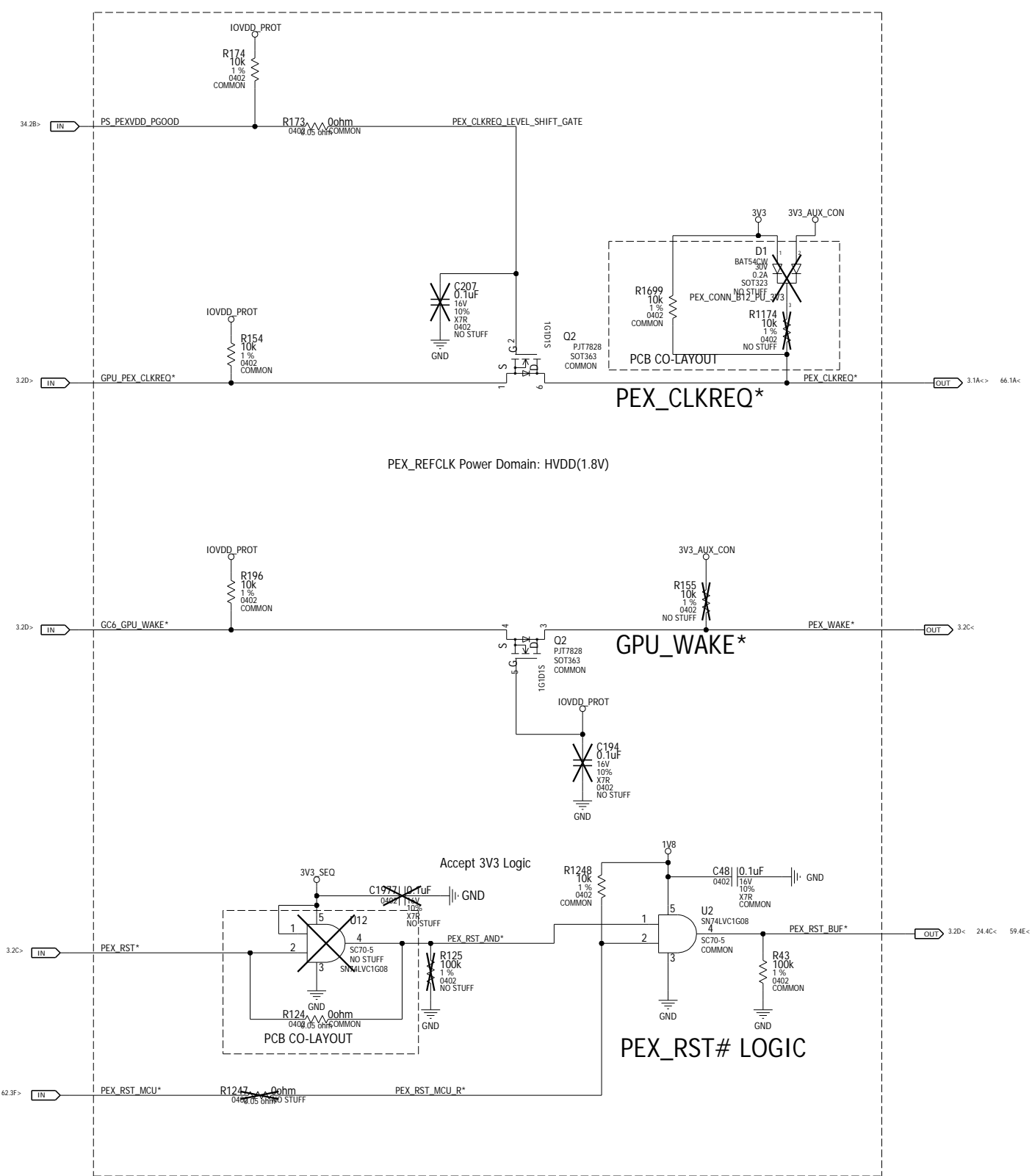
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2

2

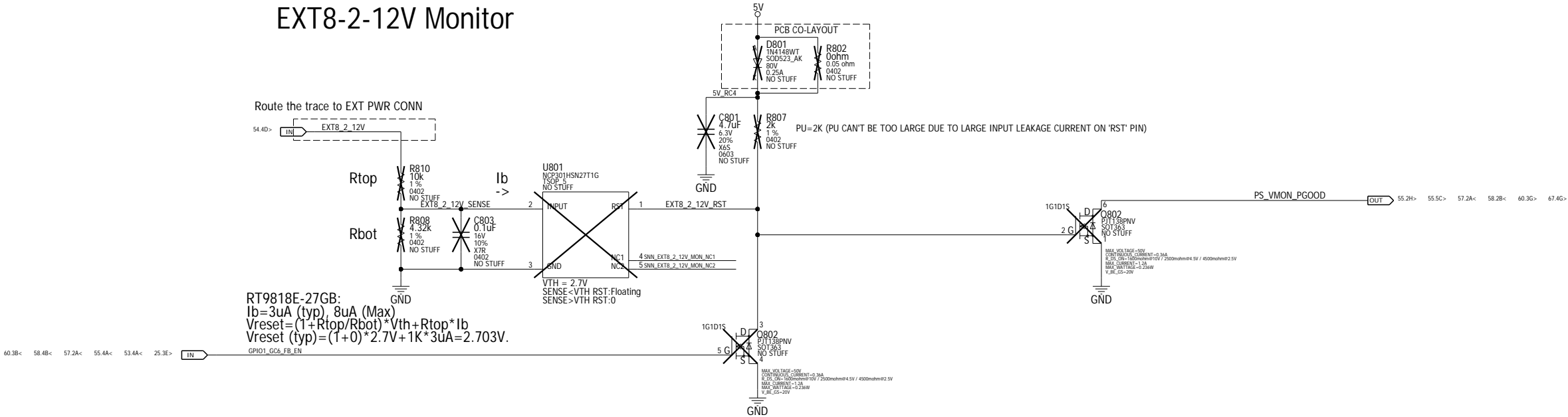


4

A

EXT8-1-12V Monitor: Co-layout with PEX3V3 Monitor

EXT8-2-12V Monitor

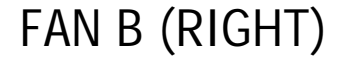




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NORTH LOGO LED (WHITE)

PCB CO-LAYOUT



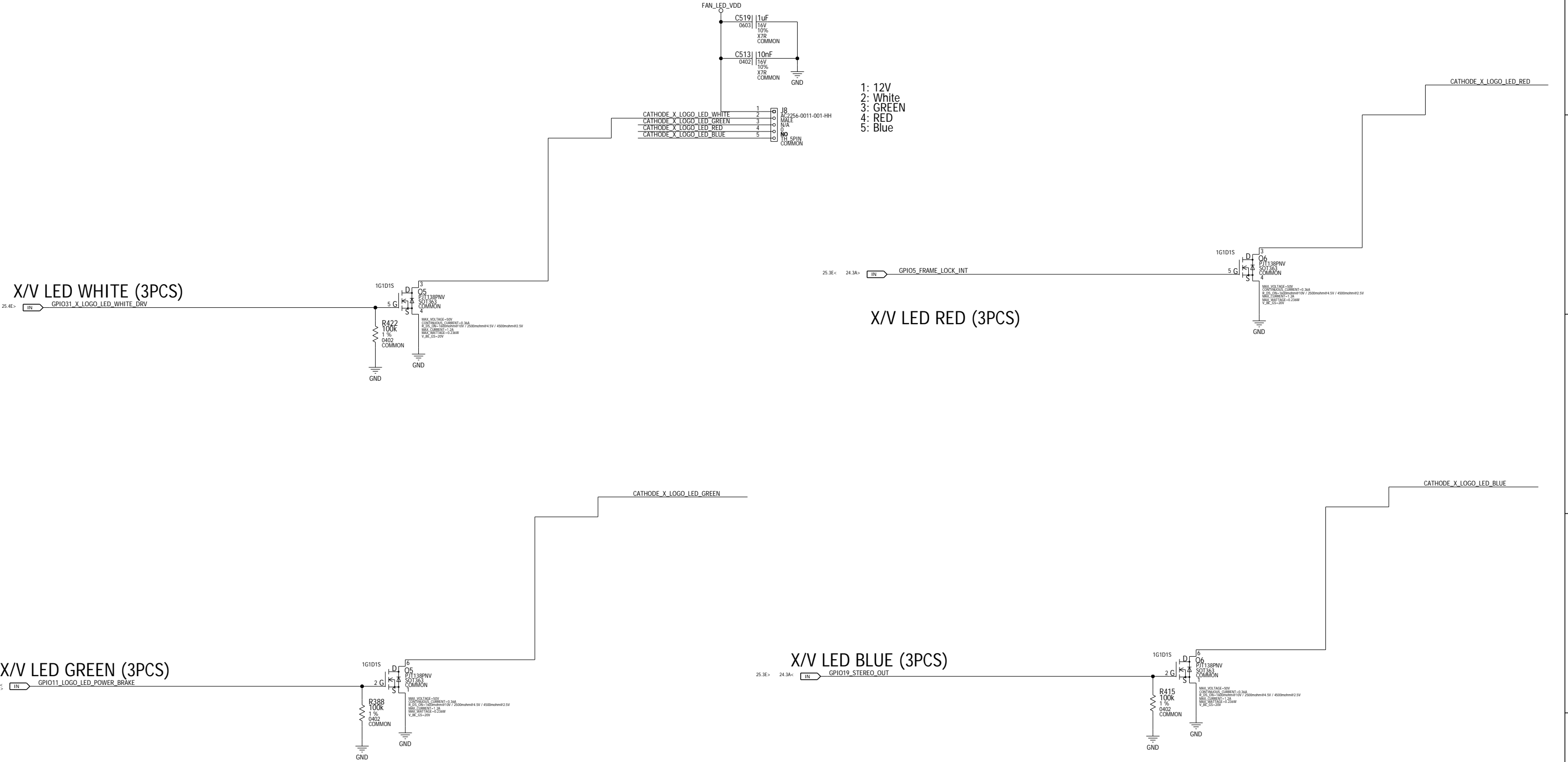
FAN A (LEFT)

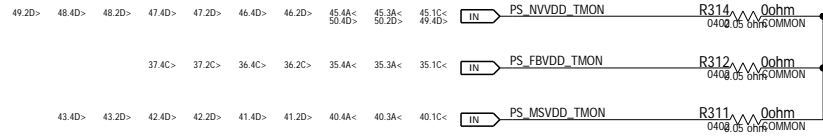


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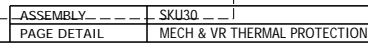
1

5-PIN POGO-PIN HEADERS FOR 'X/V' LEDS

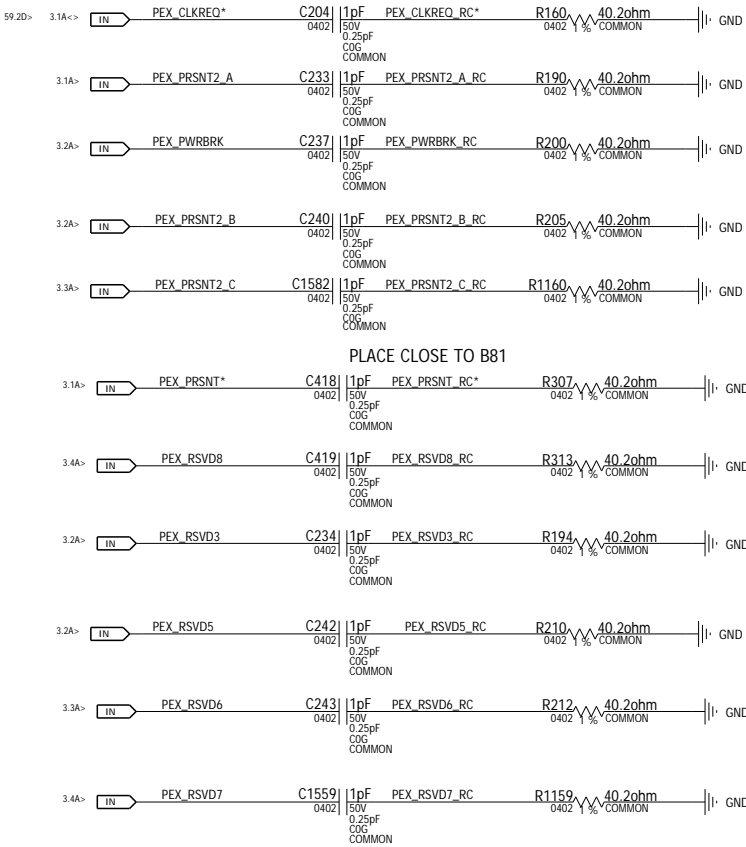




EMISTOP: 320-1764-000
TYCO: 320-1742-000



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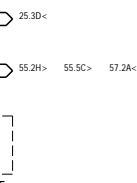
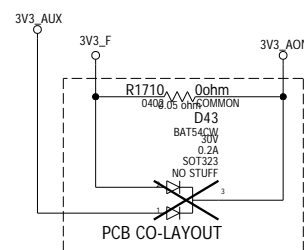
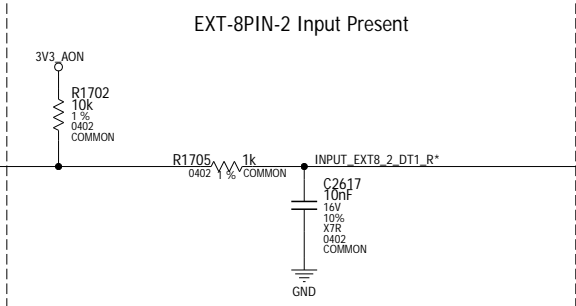
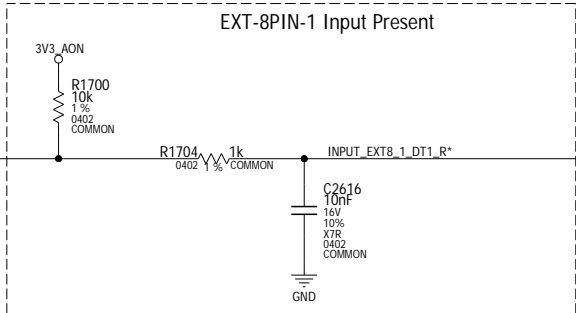
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Page 67: PRESENSE DETECT & HOT UNPLUG PROTECTION



ASSEMBLY	SKU30
PAGE DETAIL	PRESENCE DETECT & HOT UNPLUG PROTECTION

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